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Inertial Response in Virtual Synchronous Generator via Ultracapacitors

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***Abstract*—The growing penetration of converter-interfaced renewable energy sources (CI-RES) has revealed several challenges related to the stability of the electrical grids. To mitigate these issues, there is an ongoing research regarding the concept of virtual synchronous generators (VSGs), where new control schemes are employed to enable CI-RES with integrated fast-acting energy storage system (ESS) to provide ancillary services (AS) to the grid, e.g., inertial response (IR). Although several solutions have been proposed in the literature, the proper integration and energy management of the ESS towards IR provision remains an open research topic. In this paper, an holistic control approach is presented regarding IR provision by a system comprising of a CI-RES and an ultracapacitor (UC). The proposed approach is supplemented by an efficient energy management system (EMS) allowing the UC to release/absorb energy during IR provision while always ensuring the operation of the UC voltage within its technical limits. The robustness and the performance of the proposed method are experimentally evaluated in a lab setup, where all the components of the proposed system, i.e., CI-RES and UC have been analytically implemented.**

***Keywords*—Ancillary services, energy management system, experimental prototype, ultracapacitors, inertial response, virtual synchronous generator.**

I. Introduction

THE ever-increasing penetration of converter-interfaced renewable energy sources (CI-RES) with the gradual displacement of large fuel-driven power plants has brought many issues to the surface with respect to the robustness and stability of the electric power systems. Amongst them, the most important is the reduction of system inertia, [1], [2], [3], [4], which is further aggravated by the intermittent nature of the CI-RES primary source and the current control mode of the CI-RES, i.e., operation at maximum possible power. On the bright side, the continuously increasing controllability of the voltage source converters (VSCs) offers several alternatives to the CI-RES operation especially if equipped with an energy storage system (ESS). More specifically, a propitious solution that is gaining ground is the introduction of additional control algorithms into the CI-RES that mimic the behavior of synchronous generators (SGs), [3], [4], [5]. This emulation usually refers to the inertial response (IR) capability.

Various terms have been proposed to indicate CI-RES with IR capability, such as: virtual synchronous generator (VSG), virtual synchronous machine (VISMA), synchroconverter, [6]. Each solution has advantages and drawbacks as reported in [5]. Some studies propose also the inertial response (IR) provision based on the Rate-of-Change-of-Frequency (RoCoF) measurement, e.g., [7], however, such approaches include measurement delays and are not efficient, as reported by the ENTSO-E [8]. The most popular approach is the SG emulation [5] based on the swing equation, although it exhibits inherent drawbacks, such as highly oscillatory behaviour, coupling between inertial and primary frequency response, [2] and uncontrolled currents during faults, [9], [10]. For this reason, several studies have focused on improving the transient stability and the reaction of the VSG in the fault-clearing process with current limiters, [9], [10].

Another issue that has been recently reported about the IR provision is the assumption of an infinite or ideal dc source at the dc bus of the CI-RES converter. Recent research has shown that there exist a fundamental conflict between the dc-bus voltage control and IR provision, [11], [12], [13], [14] when including an actual ESS that is connected to the CI-RES dc bus via another converter (dc/dc or dc/ac). It has been proved that if an actual ESS is assumed instead of an ideal dc source, the response of the provided AS is not the “ideal" one. Therefore, there is an urgent need for including the real ESS and dc bus dynamics in the IR provision.

In the technical literature, there are studies for the IR provision considering a battery ESS (BESS), [15], a flywheel [14] or an ultracapacitor (UC), [16], [17]. However, a fast acting ESS like the UC or the flywheel would be preferred for short-term active power -related AS like IR, [18], since they possess high power density, [11]. Although these studies validate the VSG concept, most of them (especially the ones which include a UC) contain only simulation results neglecting the real dynamic conditions of the UC, e.g., the self-discharge during the AS provision. One challenge related to this issue is the need to maintain the control of the dc bus due to continuous UC discharge in order to cover the configuration system losses. Another issue is the fact that there exist technical limitations of UC energy/voltage level considering also the technical capabilities of the dc/dc converter. Therefore, the UC State-of-Charge (SoC) should be carefully designed based on this technical limitations. The effect of proper SoC recovery

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of the ESS has been studied in a limited extent including the aforementioned thoughts.

To fill the aforementioned gaps, an holistic control scheme for IR provision is proposed in this paper. The proposed system consists of a CI-RES and an UC connected to the dc bus via a dc/dc converter. Specifically, the IR control of [2] is integrated together with the energy management system (EMS) presented in [11] to properly control the UC SoC before, during, and after the IR provision. Moreover, the experimental results reveal the main shortcomings of the solutions proposed in the literature in terms of neglecting: (a) the dynamics at the dc bus of the CI-RES and (b) the limited storage capacity of fast-acting ESS. It is shown that both shortcomings are effectively addressed by the proposed holistic control scheme.

The rest of the paper is organized as follows: Section II presents the mathematical background and the main drawbacks of the state-of-the-art solutions proposed in the literature, while Section III describes the proposed holistic control scheme. Section IV presents the laboratory test bed, while Section V evaluates the performance of the proposed solution via experimental results. Finally, Section VI closes the paper with its main findings, and proposes new directions for further research.

II. VSG Model

In this section, the mathematical formulation of the VSG model proposed in [2] is briefly described. This is a modified synchronverter model presenting the following distinct advantages against the original model [19] and its variants: (a) improved damping, (b) decoupled power loops, and (c) distinct handling of IR and primary frequency response (PFR). This is attained by introducing two parallel control loops in the dc/ac VSC, i.e., the active (APCL) and the reactive power control loop (RPCL). The former is responsible for controlling the output power of the CI-RES, e.g., for IR and PFR provision, while the latter is used to provide reactive power support to the grid. Focusing on the IR provision, the output power (p_s), see Fig. 1, of the CI-RES is actively controlled by modifying the angle (θ) of the internal voltage. This is attained by introducing a proportional-integral (PI) controller as follows:

$$\dot{\theta} = k_p^f \cdot \epsilon_p + k_i^f \cdot \xi\epsilon_p \tag{1}$$

where $\epsilon_p = p_m - p_s$. Here, p_m denotes the reference active power representing the virtual mechanical power of the VSG model. Additionally, $\dot{\theta}$ is the 1^{st} derivative of θ and $\xi\epsilon_p$ stands for the integral of ϵ_p. Finally, k_p^f and k_i^f are the proportional and integral coefficients of the PI controller, respectively. The former introduces damping to the dynamic behaviour of the model, while the latter is related to the IR provision and can be determined by the inertia constant (H) using (2).

$$k_i^f = \frac{1}{2 \cdot H} \tag{2}$$

Additionally, k_p^f is calculated according to (3) in order to ensure a critically damped system, as shown in [2].

$$k_p^{f\,2} = \frac{8}{3} \cdot \frac{X_c}{E \cdot V_s} \cdot k_i^f \tag{3}$$

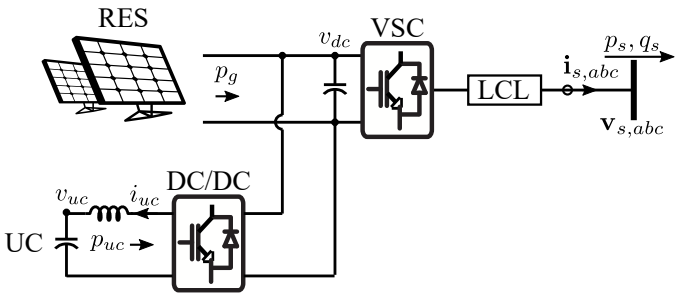

Fig. 1. CI-RES with an integrated UC at the dc bus.

Here, E and V_s stand for the voltage magnitude of the internal and point of interconnection (POI) voltage of the CI-RES, respectively, while X_c is the reactance of the output filter.

According to (1), it can be observed that during the IR provision, $\ddot{\theta}$ is non-zero leading to a power mismatch between the output power of the CI-RES (p_s) and the power generated from the primary energy source (p_m). This power mismatch is absorbed/provided by a fast ESS, e.g., an UC, located at the dc bus of the CI-RES. However, all the solutions proposed in the literature assume an ideal voltage source at the dc side of the CI-RES, neglecting the limited storage capability of UCs and the inherent dynamics at the dc side that may jeopardize the secure and reliable operatioin of the CI-RES.

RCLP aims at controlling the output reactive power (q_s) of the CI-RES by changing the magnitude of the internal voltage as follows:

$$e_q = k_p^e \cdot \epsilon_q + k_i^e \cdot \xi\epsilon_q \tag{4}$$

where $\epsilon_q = q^\star - q_s$. Here, e_q stands for q-component of the internal voltage of the dc/ac VSC in the dq reference frame, while $q^\star$ denotes the reference reactive power. Note that in the RPCL, e_d, i.e., the d-component of the internal voltage of the dc/ac VSC is considered equal to zero. Moreover, k_p^e and k_i^e are the proportional and integral terms of the PI controller, respectively, and, finally, $\xi\epsilon_q$ is the integral of the error ϵ_q.

III. UC Management for IR Provision

To overcome the above issues, the VSG model of [2] is enhanced by introducing an analytical model at the dc side of the CI-RES consisting of an UC connected to the dc bus via a step-up dc/dc converter as shown in Fig. 1. Its main scope is to maintain the voltage at the dc bus to a predefined level by covering any power mismatch between the primary energy source and the output power of the CI-RES. This is attained by implementing the cascade control scheme of [11]. This control scheme is composed of two levels: the outer voltage control loop (OVCL) and the inner current control loop (ICCL) which are analytically described below.

The OVCL consists of a PI controller with an input error $\epsilon_v = v_{dc}^{\star 2} - v_{dc}^2$ corresponding to the difference of the square of the dc bus voltage reference $v_{dc}^\star$ (desired dc bus voltage) and the actual dc bus voltage v_{dc}. The output of the PI controller is the reference current of the UC ($i_{uc}^\star$) that is forwarded to the ICCL and is computed as follows:

$$i_{uc}^\star = \frac{k_p^v \cdot \epsilon_v + k_i^v \cdot \xi\epsilon_v}{v_{uc}}, \tag{5}$$

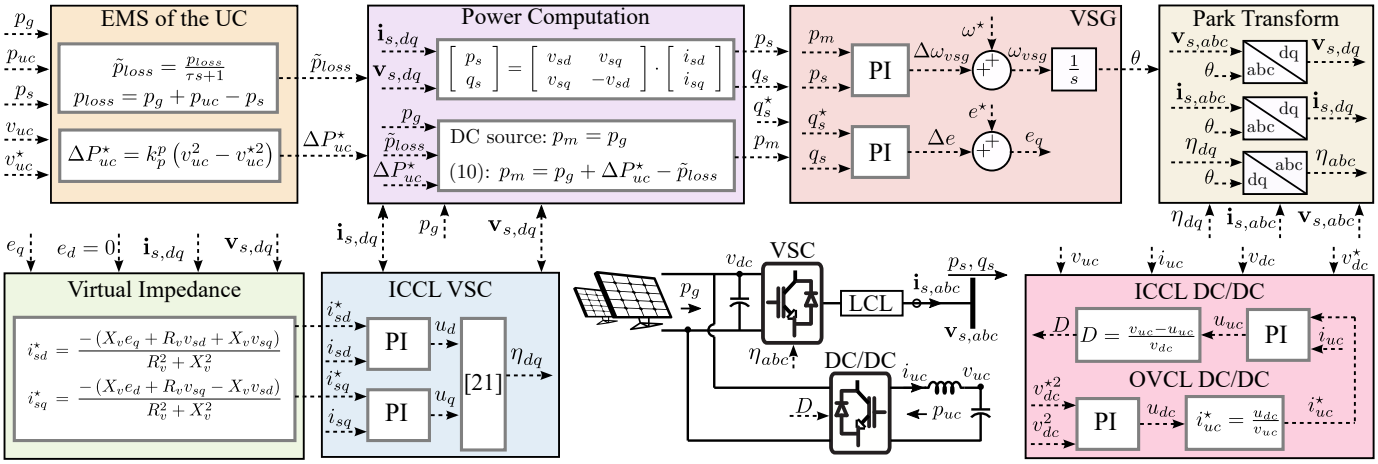

Fig. 2. Proposed cascade control scheme of CI-RES with UC.

where v_{uc} is the UC voltage, k_p^v and k_i^v are the proportional and control gains of the OVCL PI controller respectively, and $\xi\epsilon_v$ is the integral of the error ϵ_v.

Considering ICCL, a PI controller is employed to determine the duty ratio (D) for operating the dc/dc converter as follows:

$$D = \frac{v_{uc} - k_p^i \cdot \epsilon_i - k_p^i \cdot \xi\epsilon_i}{v_{dc}}, \tag{6}$$

where ϵ_i stands for the error between the reference current ($i^{\star}_{uc}$) computed by the OVCL and the actual current of the UC (i_{uc}). Furthermore, k_p^i and k_i^i are the proportional and integral gains of the ICCL PI controller respectively, and $\xi\epsilon_i$ is the integral of the error ϵ_i. Details regarding the determination of the controller gains in the OVCL and ICCL can be found in [11].

Although the above solution can actively control the voltage at the dc bus of the CI-RES by covering any power mismatch between p_m and p_s, as well as the system losses, the limited storage capability of the UCs is neglected. As a result, there is a strong possibility that the UC may fully charged or discharged, jeopardizing the operation of the whole system. To address this issue, the proposed control scheme is supplemented with an UC energy management system (EMS) aiming to control the SoC of the UC to ensure that a sufficient amount of energy can be always provided/absorbed by the UC to the dc bus. An analytical description of the EMS control scheme is presented below:

The proposed EMS method acts as a new control layer on the top of the VSG control scheme presented in Section II. Specifically, a new power reference signal is introduced ($\Delta P^{\star}_{uc}$) and calculated as follows:

$$\Delta P^{\star}_{uc} = k_p^p \cdot \left(v_{uc}^2 - v_{uc}^{\star 2}\right), \tag{7}$$

where $v^{\star}_{uc}$ is the desired UC voltage. Moreover, k_p^p is a proportional gain that is selected to recover the UC voltage back to the reference value ($v^{\star}_{uc}$). To minimize the interference between IR provision and EMS algorithm, the value of k_p^p is variable depending on the UC voltage according to:

$$k_p^p = \begin{cases} k_{p0}^p + m_{pl}^p \cdot (v_{uc}^l - v_{uc}) & v_{uc} \in [v_{uc}^{min}, v_{uc}^l] \\ k_{p0}^p & v_{uc} \in [v_{uc}^l, v_{uc}^h] \\ k_{p0}^p + m_{ph}^p \cdot (v_{uc} - v_{uc}^h) & v_{uc} \in [v_{uc}^h, v_{uc}^{max}] \end{cases} \tag{8}$$

In case the UC voltage is in a range around v_{uc}: $[v_{uc}^l, v_{uc}^h]$, a constant low value of k_p^p (k_{p0}^p) is applied, indicating a slow recovery of the UC voltage to the reference value. The values v_{uc}^l and v_{uc}^h, which define this operation range, are defined from the user according to their own technical requirements. On the contrary, voltages away from $v^{\star}_{uc}$ lead to an linear increase of k_p^p as shown in (8) to avoid over charging or over discharging the UC. In these cases, the slopes m_{pl}^p and m_{ph}^p are defined when the UC voltage is very low or very high, respectively, with the aim of restricting the energy released/absorbed by UC. Values v_{uc}^{min} and v_{uc}^{max} represent the minimum and the maximum technical value of the UC voltages. Exceeding these values may damage the UC or the system. More details of the computation of k_p^p can be found in [11].

The new reference $\Delta P^{\star}_{uc}$ is included in the calculation of the virtual mechanical power p_m as follows:

$$p_m = p_g + \Delta P^{\star}_{uc}. \tag{9}$$

where p_g is the power generated from the primary energy source. In case the UC releases energy and its voltage is decreased below $v^{\star}_{uc}$, $\Delta P^{\star}_{uc}$ has a negative value to reduce p_m. This means that part of the power from the primary source (p_g) is used to counteract the UC discharge and prevent the UC voltage from decreasing beyond its technical minimum value. If the UC voltage increases above $v^{\star}_{uc}$ due to energy absorption, $\Delta P^{\star}_{uc}$ becomes positive to increase p_m. This implies that more power is fed into the grid than is generated by the primary energy source (p_g). This extra power comes from the UC to avoid exceeding its technical maximum value.

As mentioned previously, the UC is responsible for controlling the dc bus voltage by covering any power mismatch between the primary source and the output power of the CI-RES. As a consequence, the power losses of the CI-RES setup should be covered by the UC, leading to a constant

discharging that jeopardizes the secure and reliable operation of the system. To overcome this issue and relieve the UC of this task, a new feed-forward losses compensation term ($\tilde{p}_{loss}$) is added in (9) as follows:

$$p_m = p_g + \Delta P^{\star}_{uc} - \tilde{p}_{loss}, \tag{10}$$

where $\tilde{p}_{loss}$ is computed as:

$$\tilde{p}_{loss} = p_{loss} \cdot \frac{1}{\tau s + 1} \; ; \; p_{loss} = p_g + p_{uc} - p_s. \tag{11}$$

Here, p_{loss} stands for the power losses of the CI-RES setup that are estimated according to (11). Additionally, p_{loss} is forwarded to a low-pass filter (LPF) with a time constant τ to calculate the losses compensation term $\tilde{p}_{loss}$. The LPF is introduced to add a delay in the estimation of the power losses and avoid any interference between losses compensation and IR provision. This can be attained by selecting a time constant (τ) higher than 5 s. As a result, this losses compensation technique is active during the steady-state or quasi steady-state operation of the CI-RES.

Considering the dc/ac VSC, an additional control block is added between the APCL/RPCL presented in Section II and the corresponding ICCL that computes the modulating signal η_{abc}, as shown in Fig. 2. This control block implements the concept of the virtual impedance [20] in dq reference frame using the angle θ from the APCL and is introduced to decouple the active and reactive powers, especially in low-voltage networks that are characterized by high R/X ratio. More specifically, the current references $i^{\star}_{sd}$ and $i^{\star}_{sq}$ of the ICCL of the dc/ac VSC are computed as follows:

$$i^{\star}_{sd} = -\frac{X_v \cdot e_q + R_v \cdot v_{sd} + X_v \cdot v_{sq}}{R_v^2 + X_v^2} \tag{12}$$

$$i^{\star}_{sq} = -\frac{X_v \cdot e_d + R_v \cdot v_{sq} - X_v \cdot v_{sd}}{R_v^2 + X_v^2} \tag{13}$$

where R_v and X_v are the resistance and reactance of the virtual impedance, while v_{sd} and v_{sq} are the dq components of the POI voltage. It is worth mentioning that e_d and e_q are computed by the RPCL presented in Section II.

The ICCL of the dc/ac VSC is implemented in the dq reference frame and uses two PI controllers for controlling the current i_{sd} and i_{sq} injected at the POI. This control loop follows the classical approach of the current control in VSCs [21]. The control strategy presented in Sections II and III is analytically presented in Fig. 2.

IV. Testbed Description

This section details the experimental setup used to demonstrate the effectiveness of the proposed solution towards IR provision. All the devices used in the different experiments are shown in Fig. 3. Specifically, in Fig. 3a, the configuration of the CI-RES and ESS setup is displayed consisting of a 4-leg converter. The three legs of the converter are used to build a 3-wire dc/ac VSC, while the fourth one is used as a dc/dc converter for the connection of the UC (ESS) to the common dc bus, as shown in Fig. 2. Additionally, the network coupling filters and the UC filter are displayed at the bottom of

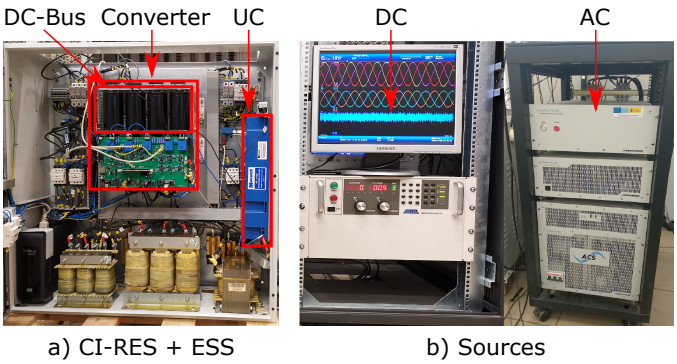

Fig. 3. Devices involved in the experimental setups

TABLE I
Parameters of Experimental Setup

Parameter	Value
DC bus voltage (v^{hv}_{dc})	730 V
RMS AC VSC rated voltage	400V
VSC rated power	20 kVA
VSC switching frequency	10 kHz
VSC side AC filter inductance (L_1)	1.25 mH
Grid side AC filter inductance (L_2)	1.25 mH
AC filter capacitance (C)	4 μF
DC/DC converter rated power	10 kW
DC/DC converter switching frequency	10 kHz
DC/DC converter filter inductance (L_dc)	3 mH
DC UC rated voltage	160 V
UC capacitance (C_{UC})	6 F
Controllable DC source rated power	30 kW
Controllable AC source rated power	40 kW

TABLE II
Controller Gains of Experimental Setup

Gains	Value
Proportional gain ICCL VSC	1.5 V/A
Integral gain ICCL VSC	160 V/A
Proportional gain VSG (k^f_p)	0.01 p.u
Integral gain VSG (k^f_i)	0.1 p.u
Virtual inertia constant (H)	5 s
Proportional gain VSG (k^e_p)	0.1 p.u
Integral gain VSG (k^e_i)	0.1 p.u
Virtual Reactance (X_v)	0.1 p.u
Virtual Resistance (R_v)	0.0 p.u
Proportional gain ICCL DC/DC converter (k^i_p)	3 V/A
Integral gain ICCL DC/DC converter (k^i_i)	120 V/A
Proportional gain ICCL DC/DC converter (k^v_p)	0.0878 A/v
Integral gain ICCL DC/DC converter (k^v_i)	0.1829 A/V
Proportional gain of the EMS (k^{p0}_p)	0.0075 W/V^2
Lower limit UC voltage (v^l_{uc})	110 V
Higher limit UC voltage (v^h_{uc})	145 V
Minimum allowed value UC voltage (v^{min}_{uc})	100 V
Maximum allowed value UC voltage (v^{mx}_{uc})	155 V
Time constant of the LPF (τ)	15 s

Fig. 3a. In Fig. 3b, the power supplies used in the experimental setup are shown. In particular, the dc/ac VSC is connected to the ac source emulating the ac grid, whereas the dc source is used as a replacement of the UC to emulate the case when an infinite source is connected to the dc bus of the dc/ac VSC. The technical parameters of these devices as well as the gains of the controllers presented in the previous sections are displayed

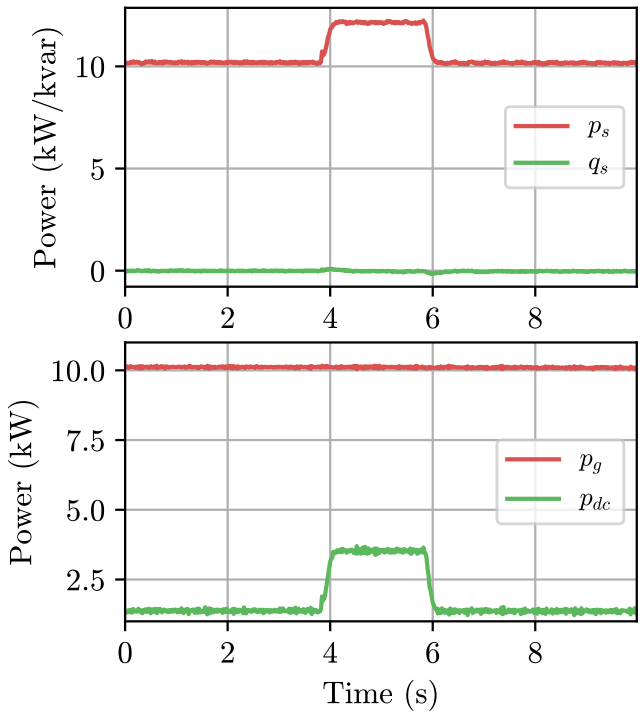

Fig. 4. Experimental results with dc source integrated in the dc bus of the CI-RES. (Top) Active and reactive power injected at the POI. (Bottom) Active power injected by the VSC emulating the primary energy source and active power delivered by the DC source.

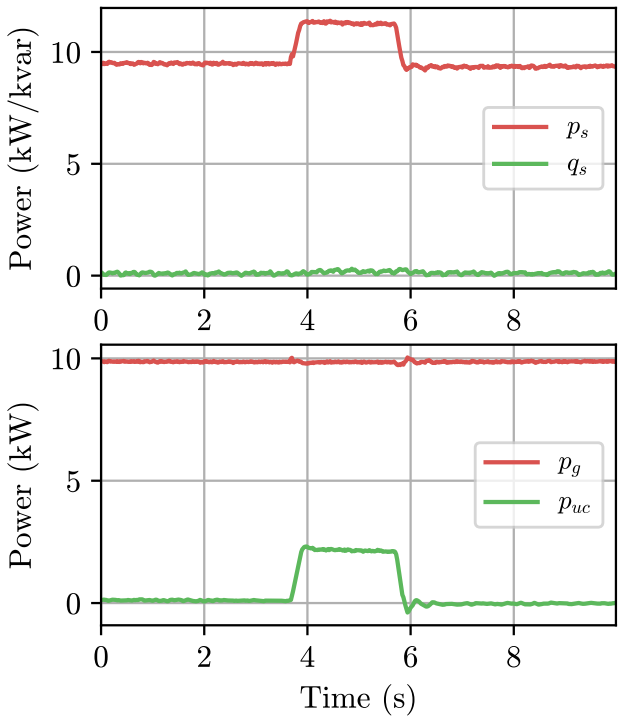

Fig. 5. Experimental results with UC and dc/dc converter integrated in the dc bus of the CI-RES. (Top) Active and reactive power injected at the POI. (Bottom) Active power injected by the VSC emulating the primary energy source and active power delivered by the UC.

in Tables I and II, respectively.

Two different configurations are examined: 1) *CI-RES + ac + dc sources* and 2) *CI-RES + ESS + ac source*. In the former case, the UC and the dc/dc converter are disabled, the dc/ac VSC is connected to the controllable ac source, and the dc bus is fed by the dc source. In this way, the performance of the CI-RES in terms of IR provision can be evaluated neglecting the limitations posed by the ESS. In this latter case, the dc source is replaced by the UC that is connected to the dc bus through the dc/dc converter. It is worth mentioning that an additional VSC is included in both configurations to emulate the primary source that feeds the dc bus, e.g., photovoltaic panels.

V. Experimental Results

To evaluate the performance of the proposed solution, the grid frequency imposed by the ac source is modified to trigger the IR provision from the CI-RES. Specifically, the frequency is reduced linearly from 50 Hz to 49 Hz in 2 s corresponding to a RoCoF of -0.5 Hz/s.

First, the performance of the *CI-RES + ac + dc sources* experimental configuration is investigated. The dc source is in charge of maintaining the dc bus voltage constant by providing the system power losses and the power needed for IR provision during the frequency reduction. In addition, p_g and $q^\star$ are set equal to 10 kW and 0 kVar, respectively.

The output active (p_s) and reactive power (q_s) of the CI-RES are presented in Fig. 4(top), while the power injected from the primary source (p_g) and the dc source (p_{dc}) are shown in Fig. 4(bottom). Initially, the power injected from the primary source is equal to the power delivered by the CI-RES at the POI since the frequency is maintained constant (50 Hz) and, therefore, the system is in steady-state condition. Nevertheless, a non-zero power is injected from the dc source (p_{dc}) which is equal to 1 kW in order to cover the system power losses. At about 4 s of the experiment, the frequency drop starts leading to an increase of p_s by approximately 2 kW, while the power supplied by the primary source remains unchanged. This extra power comes from the dc source as verified in Fig. 4(bottom). After the transient response, p_s and p_{dc} remain constant until around 6 s when the frequency drop ends and both powers return to their initial values. From this moment on, the frequency is maintained constant at 49 Hz and the output active power of the CI-RES is equal to p_g, while the dc source continues to supply the system power losses.

Assuming a 20 kVA SG with an inertia constant of 5 s, the IR towards a frequency drop with a RoCoF equal to -0.5 Hz/s can be calculated by $S_n \cdot 2H/f_n \cdot df/dt$ and is equal to 2 kW which is identical to the IR provided by the CI-RES, as verified in Fig. 4. Therefore, the proposed solution can provide IR similarly to a SG. Finally, according to Fig. 4, it can be observed that the RPCL is fully decoupled from the APCL, since the output reactive power of the CI-RES (q_s) is kept constantly equal to zero irrespectively of the output active power (p_s)

Afterward, the above-mentioned experiment is repeated to

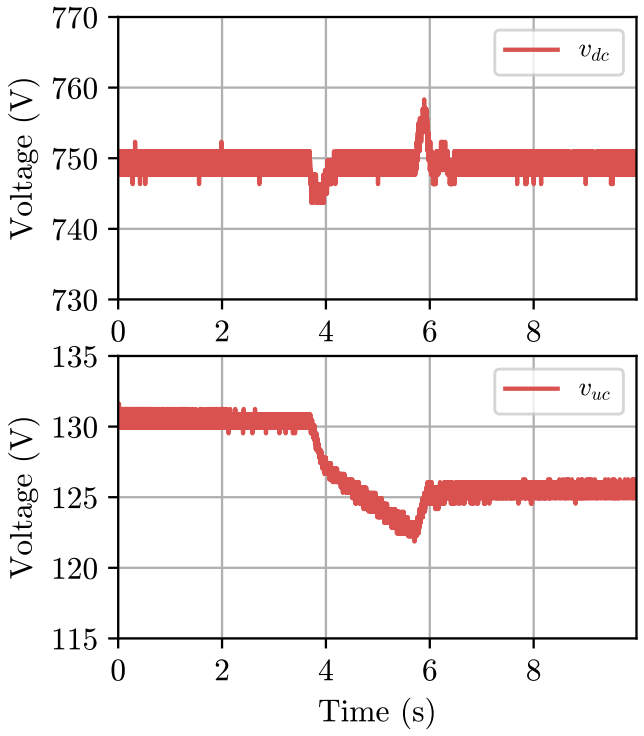

Fig. 6. Experimental results with UC and dc/dc converter integrated in the dc bus of the CI-RES. (Top) dc bus voltage. (Bottom) UC voltage.

investigate the performance of the proposed solution, namely the *CI-RES + ESS + ac source* configuration. Note that in this experiment, the UC voltage reference ($v^{\star}_{uc}$) and the dc bus voltage reference ($v^{\star}_{dc}$) are set equal to 130 V and 750 V, respectively.

The output active and reactive power of the CI-RES as well as the power delivered by the primary source and the UC are shown in Fig. 5. Initially, the system is in steady-state condition, since the grid frequency remains constant and equal to 50 Hz. However, contrary to the *CI-RES + ac + dc sources* configuration, the UC power (p_{uc}) is zero and the output active power of the CI-RES (p_s) is slightly lower than the power of the primary source (p_g). This is due to the loss compensation term introduced in (10) that forces a part of the power generated from the primary source not to be injected to the grid but to cover the system losses, thus relieving the UC from this task. Additionally, according to Fig. 6(bottom), it can be observed that the UC voltage is close to the reference value (130 V) leading to a zero $\Delta P^{\star}_{uc}$ as calculated by (7). Furthermore, the dc bus voltage is kept close to the reference value (750 V) as shown in Fig. 6(top), indicating the robustness of the proposed cascade control scheme.

At around 4 s, the frequency drop starts leading to an increase of the p_s by 2 kW, which is provided by the UC as shown in Fig. 5(bottom). Nevertheless, the IR differentiates from the corresponding resulted from the *CI-RES + ac + dc sources* configuration. Specifically, the IR provision leads to a UC discharge, which is also reflected in a reduction of its voltage as illustrated in Fig. 6(bottom). This implies that $\Delta P^{\star}_{uc}$ is non-zero, which, in turn, reduces p_m according to (10). Therefore, p_s and p_{uc} are progressively reduced according to the $\Delta P^{\star}_{uc}$ during the frequency drop. Note that the UC voltage is within a safe range v_{uc}: $[v^{l}_{uc}, v^{h}_{uc}]$ (see Table II and (8)) which corresponds to a low value of k^{p}_{p} and $\Delta P^{\star}_{uc}$. In this range, the UC energy release is prioritised to provide IR over maintaining its SoC. The impact of $\Delta P^{\star}_{uc}$ in p_s and p_{uc} is clearly observed in Fig. 5 during the frequency drop. However, these values decrease with a low slope ramp because $\Delta P^{\star}_{uc}$ is relatively small in this range of UC voltages, as shown in (8).

After the end of the frequency drop, around 6 s, the frequency is kept constant at 49 Hz and the powers return approximately to their original values. Again, there are differences with respect to the *CI-RES + ac + dc sources* configuration. Specifically, p_s is slightly lower than before the frequency drop. Similar behaviour is reflected in p_{uc}, reducing its value with respect to the original value. This is due to two reasons. Firstly, p_m is affected by loss compensation due to the increase in power during the frequency drop. This compensation occurs with a delay due to the LPF applied to the power losses. Secondly, the UC voltage is reduced to 122 V, therefore, it is restored to the reference voltage by the action of the $\Delta P^{\star}_{uc}$. This recovery is slow since the UC voltage is within the safe zone as discussed above, and it increases progressively as shown in Fig.6 after 6 s.

Finally, it is worth mentioning that the dc bus voltage is hardly affected by active power p_s variations. since it varies less than 10 V, indicating a fast response and robust performance of the dc bus voltage controller in the transient regime. Furthermore, p_g is slightly modified during the increments and decrements of p_s. This is because this power is computed from the dc bus voltage and the current injected from the VSC emulating the primary power source. Therefore, the voltage swing of the dc bus is reflected in this power.

VI. Conclusions

In this paper, a holistic approach has been presented regarding the IR provision by a system consisting of a CI-RES, emulating a VSG, and a UC as an ESS. The UC is connected to the CI-RES dc bus via a dedicated dc/dc converter. It is proposed that the UC controls the dc bus voltage of the system to provide energy required for IR in a natural way from the CI-RES. For this purpose, a cascade control to control the dc bus voltage through the current circulating from the UC is implemented. In order to avoid excessive charging or discharging of the UC, a EMS is proposed which modifies the mechanical virtual power of the VSG by adding a term corresponding to the power losses compensation of the converters and a proportional control in charge of controlling the UC voltage. This control adjusts its gain as a function of the UC voltage in order to release its power or restrict it in case it is close to unwanted technical values of the UC voltage.

The proposed control scheme is validated via experiments in a real lab prototype and involves two stages: *(a)* an ideal dc source is connected to the dc bus; *(b)* an actual commercially available UC is employed to provide IR. Experimental results reveal that the CI-RES emulating a VSG with a dc source is able to provide IR to the grid during frequency events

according to a specified value of inertia constant. Furthermore, an adequate decoupling with reactive power is achieved thanks to the introduction of a virtual impedance in the controller. The experimental results for the UC show that the ability to supply IR is slightly reduced with respect to the dc source case. This is thanks to the EMS which simultaneously allows to provide a quality IR while the UC voltage is maintained within adequate limits before, during and after the IR.

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