Citation Information: DOI: 10.1109/TIA.2022.3195975

Ramp-Rate Limitation Control of Distributed Renewable Energy Sources via Supercapacitors

Kyriaki-Nefeli D. Malamaki, *Member, IEEE*, Francisco Casado-Machado, *Student Member, IEEE*, Manuel Barragán-Villarejo, Andrei Mihai Gross, Georgios C. Kryonidis, *Member, IEEE*, Jose Luis Martinez-Ramos, *Senior Member, IEEE*, Charis S. Demoulias

***Abstract*—The growing penetration of Converter-Interfaced Distributed Renewable Energy Sources (CI-DRES) has posed several challenges into the electric power systems, e.g., the instability caused by the intermittent nature of the primary sources, power quality issues, etc. Several algorithms have been proposed to mitigate the CI-DRES power fluctuations and reduce high active power ramp-rates (RRs) at the Point of Common Coupling (PCC) with the grid using energy storage systems (ESS). However, these algorithms present some drawbacks. In this paper, a new Ramp-Rate Limitation (RRL) control method is proposed to address existing gaps in the technical literature. This algorithm is performed considering the connection of a Supercapacitor (SC) at the DC-link of a DRES converter. The relationship between the SC voltage and the degree to which the RRL is achieved is established, aiming to reduce the SC voltage fluctuations and increase the SC life time. The RRL control is validated in a real experimental testbed and compared to state-of-the-art approaches. This control is also modelled in Matlab/Simulink in order to perform techno-economic investigations on the influence that several parameters (SC size, SC charging/discharging cycles, cost, etc.) have on the achieved RRL at the DRES PCC.**

***Index Terms*—Distributed Power Generation, Energy Storage Systems, Power Smoothing, Ramp-Rate Control, Renewable energy sources, Supercapacitors, Safety, Ultracapacitors, Voltage Source Converter.**

I. Introduction

THE advent of Renewable Energy Sources (RES) and power electronics in conjunction with the simultaneous gradual replacement of fuel-driven power plants (PPs) has initiated a new, environmentally friendly era for the electric grid. However, this shift towards a decentralized non-synchronous generation jeopardizes the security, robustness and stability of power systems, [1]. For these reason, huge amounts of units are committed as spinning reserves. To mitigate the problem of excessive unit commitment, many grid codes are posing specific limits to the Ramp-Rates (RRs) of RES PPs directly connected to the Transmission System (TS), [2], [3]. In most cases, it is assumed that only ramp ups can be easily mitigated via Active Power Curtailment (APC). The ramp downs cannot be tackled since no Energy Storage Systems (ESS) are mandated. The APC action for the RR Limitation (RRL) is an undesired function due to revenue loss for the RES PP owners. The growing number of Distributed RES (DRES) in distribution systems (DSs) also leads to high DRES RRs, which in turn cause power quality issues within DSs, e.g., voltage rise and flickering. One solution to compensate the DRES impact on the dynamic performance is the placement of central large-scale ESS at the Point of Interconnection (POI) of the DS with the TS or within a large-scale RES PP, [4], by providing ancillary services (AS). However, this approach has high cost, and the stakeholders involved are TS Operators (TSOs), DS Operators (DSOs) or large energy market players. Hence, small DRES owners are not able to participate in a respective market. In addition, the grid codes and standards do not provide specifications for RES PPs with nominal power below $1MW$. Therefore, the ability of DRES located within DSs to provide RRL as an AS remains untapped.

Another issue is that currently numerous specifications exist with respect to the RR time interval Δt (usually 1 or 10 minutes, [2]) or the RES power variation ΔP, hence, there is no unified approach for the definition of the RR. In the literature, three different methods have been identified, [5], however, the most preferable one is the difference between two successive time instants, which is more suitable for high-frequency fluctuations at DRES level, [5], due to the fast nature of the primary source (cloud movement, wind).

In the recent literature, there exist several methods to mitigate the fluctuations at DRES level or microgrid level considering different limits of RR depending on the type of the primary source (sun, [6]–[9] or wind [10], [11]) and different types of ESS: Supercapacitors (SCs), [12], Battery ESS (BESS), [7], [8], [10], [13], or even hybrid ESS (HESS), [11], [14], which consist of a fast acting ESS, e.g., a SC, and a slower ESS, e.g., a BESS. An extensive review on the control methods exists in [1], [15], [16]. The RRL methods can be generally categorized as:

(i) moving average (MA) methods [5], [6], where the previous DRES active power values are averaged for a given window of time, which may vary from 1 to 10 minutes.

(ii) filter-based approaches, [7], [10], [11], where the input DRES power is passed through a filter with a user-defined time constant, [16]. The value of the time constant is re-evaluated until smoother waveform of DRES power is produced, [16]. The most popular filter-based method is the application of a Low-Pass Filter (LPF), [7]. The drawback of such an approach is that there is no correlation of the filter time constant with the achieved RRL. In addition, in [7] the LPF control is applied to a BESS and is disabled if the State-of-Charge (SoC) is above 80% or below 20%. It is concluded that during 11.00-14.00 hours the LPF cannot mitigate high PV fluctuation if the ESS capacity is fully exhausted - below 20%. This issue could be solved only if there was a continuous interaction

Manuscript received June 4, 2022

and adjustment of the ESS SoC and the requested RRL. However, with this LPF method the achieved RRL cannot be pre-evaluated - on the contrary the PV power is smoothed even when not required (oversmoothing). This is the reason behind the full exhaustion of the ESS SoC with this approach.

(iii) direct RRL methods: the rate of change or slope of the injected power is limited when a pre-determined RRL is violated, [12], [16]. Such methods are presented in [8], [9], [14], [17], [18].

The MA and the filter-based approaches present some disadvantages, [1], [16], e.g., high computational complexity, exhibition of "memory effect" and oversmoothing. The latter causes the following impacts: (a) the ESS is forced to operate even when the DRES RR is within specific limits; (b) the ESS capacity is increased; (c) the ESS operating life is decreased. In the technical literature there exist several comparison studies for BESS [8], [13], [19] and SCs, [12], [20], in order to support the superiority of the direct RRL strategies against MA (sliding window and/or exponential) and filter-based approaches (especially, the LPF approch, [7]). In all these studies, the conclusion is that the direct RRL methods outperform the MA and the filter-based methods, [1], [16], since they eliminate the "memory effect" and most importantly, could guarantee a specific RRL at DRES level. The direct RRL methods lead to reduced ESS size, since the ESS does not operate unnecessarily.

In [18] the application of MPPT based RR algorithm is proposed and the PV converter is controlled to curtail power during ramp-ups in order to prolong the BESS life. However, this approach leads to PV APC, hence, revenue loss to the owners, and cannot guarantee to control the RR within the prescribed level. Moreover, the PV APC will incur high energy losses due to inverter power limitation than other direct RRL control methods, [16]. In the direct RRL approach of [8], the PV output RR is limited by following an inverse characteristic of the desired RR with the PV RR during the ramping event. The examined ESS is a lead-acid BESS. When the ramping event is over, the direct RRL is switched to a droop characteristic to restore the SoC. In all these direct RRL methods the SoC is taken into account *a-posteriori*, i.e., after the power smoothing action, [1], [16]. Therefore, it is not guaranteed that the RR can be limited exactly to the prescribed level, because the ESS may reach its SoC limits unexpectedly, [16]. This unexpected pause of the power smoothing action could cause further unexpected ramps, instead of remeding the high DRES RRs. In [16] it is recommended that new direct RRL techniques should be developed mitigating significant RRs and considering the ESS SoC before the ESS capacity is exhausted. Mitigating the RR to the prescribed level is crucial in order to avoid voltage and frequency fluctuations at the grid side, [16]. It should be noted that in these studies: (a) the problem of oversmoothing is not addressed clearly, [16]; (b) a fixed RRL of $10\%/min$ is assumed based on Puerto Rico Electric Power Authority (PREPA) regulations, [1]. However, it has been suggested by PREPA, [4], that the $10\%/min$ rule for the RRL should be re-assessed due to high costs.

The aforementioned direct RRL methods have been applied to BESS. However, in [4] it has been proven that the BESS is too slow to follow the cloud movement (in the case of PV PPs), hence it is not suitable for high-frequency fluctuations at DRES level, [1], [16]. For this reason, in [12], [16] it is recommended that fast-acting ESS, especially SCs, are used for DRES power smoothing in DSs, since the SCs are faster than BESS, have longer useful life and are economically profitable for small scale systems. In [12] the sliding window MA [16], the LPF approach of [7] and the direct RRL approach of [18] are applied to small-scale PV system (15kW) coupled with SC assuming solar irradiance in an Andean city. The methods are compared only via time domain simulations in order to evaluate the charge/discharging cycles of a specific SC size to limit the RR at $10\%/min$.

This paper proposes a new direct RRL algorithm so as to reduce the high-frequency fluctuations of DRES using a SC as an ESS. The developed algorithm aims to eliminate the "memory effect" and oversmoothing. An important aspect of the developed control, is that it does not use any filter or any averaging function for deriving the smoothed power reference signal, but it directly restricts the power RR to a desired maximum value using the direct correlation with the $\Delta P/\Delta t$. This is important because, all grid codes on RRL/power smoothing are expressed by a $\Delta P/\Delta t$. Therefore, although there is no clear definition for the RR and different Δt might lead to different RR calculations, using the RR as a parameter within the control strategy, makes it directly applicable to all requirements. In addition, the proposed control has been implemented using basic arithmetic operations and the RR computation is performed using only the previous value, i.e. the RR is calculated based on the difference between two points, [5], in order not to increase the computational burden. This makes the proposed RRL method directly applicable to any DRES converter as well, which is another clear advantage with respect to the above approaches. The low computational cost and the limited memory requirement of the proposed approach is also an advantage compared to MA or filter-based approaches, especially, if the RRL is to be provided together with other AS due to the fact that it does not overload the Digital Signal Processors (DSPs) of the CI-DRES VSCs.

The degree to which the ESS can fulfil a pre-defined RRL as an AS depends on its SoC. Since in all the aforementioned studies, the SoC is taken into account only *a-posteriori*, the ESS cannot achieve the requested RRL, when the SoC reaches its limits. For this reason, in this paper the proposed RRL control considers the SC SoC (i.e. the SC voltage level) *a-priori*: depending on the SC voltage, the RRL control is continuously adjusted in order not to exhaust the SC technical limits recommended by the manufacturers. Such method ensures that the RR is limited exactly to a pre-determined value, something that is missing from the literature, [16]. This is important if a CI-DRES provides RRL as an AS at a specific DSO/TSO value and the DRES owner is remunerated for this AS. Such proactive SC SoC control and interaction between SC SoC and RRL allows the combined system of CI-DRES/SC to perform not only RRL at a specific pre-defined value or specific range of values, but also multiple AS related to short-term active power. In addition, it is shown that this *a-priori* correlation between the SC SoC and the requested RRL can: (i) lead to

reduced SC size and ensure smoother grid injected power with a specific pre-defined RRL (or within a specific pre-defined range of RRL values); (ii) **simultaneously** ensure a safer SC operation for a given SC size compared to the case where other control approaches are applied and, the SC size is not large enough and in turn, the power smoothing functionality is disabled when the SC reaches its limits. Such case could cause further undesired effects at power system level.

Besides its theoretical contribution, this paper has additional experimental contribution: The proposed approach is compared to the LPF method of [7] and the sliding window MA via experiments in a 3-phase $20kVA$ DRES Voltage Source Converter (VSC) prototype connected to a commercially available SC of $6F/160V/21.33\ Wh$, [21] via a dedicated bi-directional DC/DC converter. The comparison is performed in terms of the achieved RRL and SC cycles (via the SC voltage). It is noted that such experimental comparison studies do not exist in the technical literature. Finally, this paper has additional contributions compared to [1]:

(i) The SC SoC recovery within the experiments and the simulations is performed using the control scheme presented in [22], while in [1] the SC recovers its SoC based on the control presented in [23]. The energy recovery of the SC is improved with the control scheme presented in [22], because the controller gains have been decided based on the capacitors' energy content (the SC and the DC-link one), while in [23] these gains were determined via trial-and-error. In this way, the control scheme of [22] leads to better dynamic performance of the DC-link and SC voltage control.

(ii) A performance/size/cost comparison is performed among the proposed RRL control, the LPF, [7] and the sliding window MA. This comparison involves two stages: a) experimental results using a step profile and considering the same size of SC and different values of LPF time constants, as well as the MA approach with the maximum possible window selected as not to overload the VSC DSP; b) simulation results considering different values of the SC size, the LPF time constants and MA sliding window lengths. One additional comparison is performed for the evaluation of the cost/size of the SC: when a SC purchase cost limit is imposed, its impact on the achieved RRL, the SC cycles during a day and the SC recovery time is examined. In addition, the issue of the appropriate RRL for DRES within DS is discussed.

The rest of the manuscript is organised as follows: Section II presents the proposed RRL control. Section III describes the prototype used for the experimental validation of the control strategy and presents experimental results in comparison also with the LPF and MA control methods. In Section IV simulation results are presented, which allow for further investigations on the effect of different parameters and evaluates all three control approaches in a techno-economic manner. Finally, Section V closes the paper with its main findings, discusses the results in comparison with the state-of-the-art techno-economic studies for the power smoothing strategies and proposes new directions for further research.

II. Proposed Methodology

A. Converter/ESS Configuration

The studied topology is a CI-DRES that is interfaced with the grid via a three-phase, three-leg DC/AC VSC, as illustrated in Fig. 1. The voltage of the VSC DC-link is controlled by the SC and the associated bidirectional DC/DC converter. The primary source is connected to the DC-link via an Maximum Power Point Tracking (MPPT) device (not shown in Fig. 1). The whole converter was developed and tested in the frame of the H2020 EU funded project EASY-RES, [24]. A hierarchical control structure composed of three levels has been used the details of which can be found in [22] and [25]. In this subsection the first two control levels (CTRLs) are described briefly while the third CTRL that affects the proposed RRL control is presented in more detail.

The three-level hierarchical control structure is composed by: SC current control level (CTRL1), DC-link voltage control level (CTRL2) and SC voltage control level (CTRL3). The CTRL1 and CTRL2 control the VSC DC-link voltage through a classic cascade control, while CTRL3 aims to maintain the SC voltage, thus, its SoC, within the technical limits recommended by the SC manufacturer. At the same time CTRL3 must not interfere with the power required by the AS, p_{AS}. Therefore, CTRL3 has to satisfy two objectives that in principle can be considered opposed: absorb or inject energy to keep the SC voltage within technical limits and release its energy during the provision of the AS. Each CTRL and the interfaces among them are analyzed below:

1) Current control level (CTRL1): The input of CTLR1 is the current reference $i^{\star}_{\text{SC}}$ generated by CTRL2. The scope of CTRL1 is to generate the DC/DC converter duty cycle D. A proportional and integral (PI) controller is implemented for this purpose designed from the DC/DC converter average model and the voltage drop between the SC and the converter. Further details on the computation of D can be found in [22].

2) DC link voltage control level (CTRL2): CTRL2 aims is to control the voltage of the VSC $v_{\text{DC-l}}$ and calculate the reference SC current $i^{\star}_{\text{SC}}$. Further details can be found in [22].

3) SC voltage control level (CTRL3): CTRL3 is based on the **power balance** of the total set-up in Fig. 1:

$$p_s = p_{\text{SoC}} + p_{\text{in}} + p_{\text{AS}} - p_{\text{loss}} \tag{1}$$

where p_{SoC} is the SC SoC recovery active power, p_{loss} are the total power losses and p_{AS} is the power required during the AS - it is set to 0 during steady-state conditions. If the primary active power p_{in} is injected into the grid by the VSC ($p_s = p_{\text{in}}$), the SC has to cope with p_{loss}. Nevertheless, if the power balance between p_s and p_{in} is not achieved due to the provision of an AS involving active power (like RRL), the SC injects the power required for the AS p_{AS}, because the SC is in charge of controlling $v_{\text{DC-l}}$. Therefore, the SC power must supply at least $p_{\text{SC}} = p_{\text{AS}} + p_{\text{loss}}$, i.e., the SC should also take care of p_{loss}. In this case, the SC is continuously subjected to charging and discharging processes. For this reason, the SC should properly recover its SoC besides the AS provision. In order to enable the proper control of $v_{\text{DC-l}}$ it is suggested in

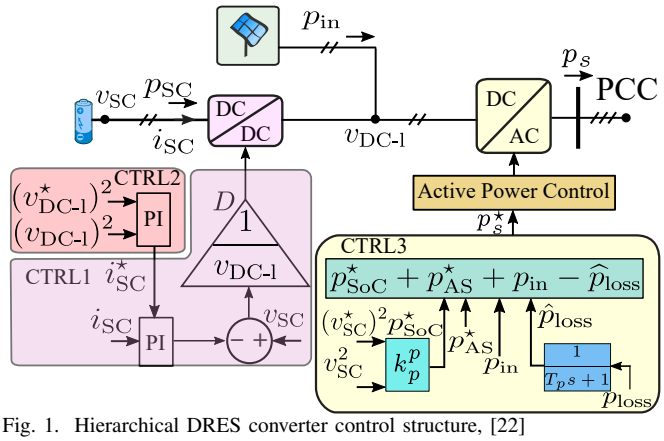

Fig. 1. Hierarchical DRES converter control structure, [22]

[22] that the VSC reference power at the DRES PCC $p_s^\star$ is computed in CTRL3 as:

$$p_s^\star = p_{\text{AS}}^\star + p_{\text{in}} + p_{\text{SoC}}^\star - \hat{p}_{\text{loss}} \tag{2}$$

where $p_{\text{AS}}^\star$ is the reference signal corresponding to the provided AS, i.e., RRL, and is given by the RRL control described in **Algorithm 1** in the following subsection. The power losses can obtained indirectly by measuring p_{in}, p_{SC} and p_s:

$$p_{\text{loss}} = p_{\text{SC}} + p_{\text{in}} - p_s \tag{3}$$

In [22] it is suggested that a LPF is used to be applied in p_{loss} acting as a feed-forward signal ($\hat{p}_{\text{loss}}$) that causes the power losses compensation to be provided by the VSC instead of the SC in steady-state conditions. In this way, both the AS provision and the DC link voltage control are not affected, [22]. The parameter $\hat{p}_{\text{loss}}$ is calculated by:

$$\hat{p}_{\text{loss}} = p_{\text{loss}} \frac{1}{T_p s + 1} \tag{4}$$

The time constant T_p must be selected with a value higher than the duration time of the AS to avoid large interference in the power supplied for the AS, [22].

The term $p_{\text{SoC}}^\star$ is in charge of restoring the SC SoC, [22] and is calculated based on a proportional controller and the difference between the voltage squares:

$$p_{\text{SoC}}^\star = k_p^p \cdot \left[(v_{\text{SC}})^2 - (v_{\text{SC}}^\star)^2 \right] \tag{5}$$

where $v_{\text{SC}}^\star$ is the reference SC voltage. In order to respect the SC voltage and energy limits given by the manufacturer for safety reasons, the calculation of $p_{\text{SoC}}^\star$ in (5) and $p_{\text{AS}}^\star$ (presented below) takes into account that the SC SoC should be correlated with the SC energy content and respective voltage levels, [26]. This correlation is expressed by:

$$\text{SoC} = \frac{v_{\text{SC}}^2 - v_{\text{min}}^2}{v_{\text{max}}^2 - v_{\text{min}}^2}, \tag{6}$$

where v_{max} and v_{min} the technical operational limits of the SC recommended by the manufacturer. The SC rated energy is $E_{\text{rated}} = 0.5 \cdot C \cdot v_{\text{max}}^2$, while the "used" SC energy based on these limits is equal to:

$$E_{\text{used}} = 0.5 \cdot C \cdot (v_{\text{max}}^2 - v_{\text{min}}^2) \tag{7}$$

Since the degree to which the SC can fulfil an AS depends on the SC voltage level and the associated energy content, the term $p_{\text{AS}}^\star$ is continuously adjusted every time instant for the provision of RRL considering the SC SoC *a-priori*. This is achieved by computing the RRL value as a function of the SC voltage, as described in the next subsection.

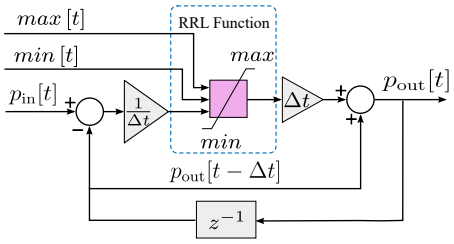

Fig. 2. Dynamic RRL

B. RRL Control

In this subsection, the proposed RRL control for the injected active power at DRES PCC, p_s is described. It is considered that both ramp-ups and ramp-downs should be mitigated, hence, the SC should be charged at approximately 50% of the available energy to be used, E_{used}. The RRL control corresponds to the computation of the term $p_{\text{AS}}^\star$ that is sent as input to CTRL3. As mentioned above, the degree to which the SC can fulfil a pre-defined RRL r_n (sent by a DSO or a TSO) as an offered AS depends on the SC SoC, i.e., its voltage level. In case the SC SoC is above or below certain limits, then it can not provide the requested r_n for specific time intervals within a day, i.e., the RRL can be continuously enabled/disabled. This situation could create more issues at power system level, instead of resolving them. For this reason, in this paper it is suggested that the SoC is considered *a-priori*, i.e., the RRL value is continuously adjusted as a function of the SC voltage, v_{SC}. Such proactive SC SoC control allows the combined system of CI-DRES/SC to perform multiple AS in addition to RRL, e.g., virtual inertia. As it can be deduced from the above expressions, there is a continuous trade-off between $p_{\text{AS}}^\star$ and $p_{\text{SoC}}^\star$ in (2). If v_{SC} is close to $v_{\text{SC}}^\star$, it means that there is no need to recover the SC SoC and $p_{\text{SoC}}^\star$ has a really small value. On the contrary, there is enough SC power capacity to provide $p_{\text{AS}}^\star$ and perform the RRL control.

The RRL function performed in the pink block of Fig. 2 is described via **Algorithm 1**. The RRL control is performed based on the RRL calculation given by (8) every Δt, i.e., RR definition between two successive instants, [5].

$$RR_{\text{2-point-calc}}[t] = \frac{p_{\text{out}}[t] - p_{\text{out}}[t-\Delta t]}{t[t] - t[t-\Delta t]} \tag{8}$$

Algorithm 1 Algorithm for RRL Function

Require: $p_{\text{in}}[t]$, $p_{\text{out}}[t-\Delta t]$, $min[t]$, $max[t]$, Δt
Ensure: $p_{\text{out}}[t]$, $p_{\text{SC}}^\star[t]$

$RR_{\text{2-point-calc}} \leftarrow \dfrac{p_{\text{in}}[t] - p_{\text{out}}[t-\Delta t]}{\Delta t}$
if $RR < min[t]$ **then**
  $RR \leftarrow min[t]$
else if $RR > max[t]$ **then**
  $RR \leftarrow max[t]$
else
  $RR \leftarrow RR_{\text{2-point-calc}}$
end if
$p_{\text{out}}[t] \leftarrow RR \cdot \Delta t + p_{\text{out}}[t-\Delta t]$
$p_{\text{AS}}^\star[t] \leftarrow p_{\text{in}}[t] - p_{\text{out}}[t]$

The inputs are the DRES power, $p_{\text{in}}[t]$, the maximum ($max[t]$) and minimum ($min[t]$) limits of RRL considering

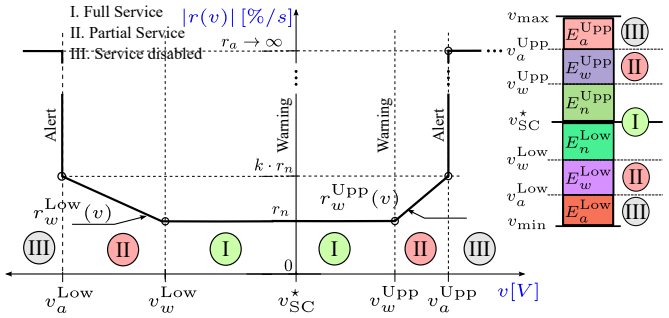

Fig. 3. RRL Function: SC voltage versus the absolute value of RRL.

both ramp-ups and ramp-downs. These limits are not constant; on the contrary, they are evaluated every Δt and defined by the RRL Function block (Fig. 3) and are $max[t] = +r(v)$ and $min[t] = -r(v)$ - to be explained. The output of the control block is the smoothed power $p_{\text{out}}[t]$ and is calculated in line 9 of **Algorithm 1**. The value $p_{\text{out}}[t - \Delta t]$ is defined by a Unit Delay block z^{-1}, which holds and delays its input by a user-defined sample period Δt. The term $p^{\star}_{\text{AS}}[t]$ is determined in line 10 of **Algorithm 1** as the difference between $p_{\text{out}}[t]$ and $p_{\text{in}}[t]$ corresponding to the power needed from the SC in order to perform RRL. In this way, $p^{\star}_{\text{AS}}[t]$ is inserted in the power balance of (2) in CTRL3.

The values of $min[t]$ and $max[t]$ are determined based on the SC voltage v_{SC} every Δt. The interdependence between these limits and v_{SC} is illustrated graphically in Fig. 3. The diagram correlates the adjustment of $min[t]$ and $max[t]$ as a function of v_{SC}. More specifically, based on the v_{SC} measurement, $max[t] = +|r(v)|$ and $min[t] = -|r(v)|$ are continuously re-adjusted. Three voltage areas are distinguished. These areas are determined actually by the split of the total SC E_{used} into respective areas. The column next to the diagram in Fig. 3 denotes the SC energy areas. The SC energy Area I corresponds to the sum of $E_n^{\text{Low}} + E_n^{\text{Upp}}$ and the SC voltage Area I corresponds to the region $v_w^{\text{Low}} - v_w^{\text{Upp}}$. The SC energy Area II corresponds to the sum of $E_w^{\text{Low}} + E_w^{\text{Upp}}$ and the SC voltage Area II corresponds to the region $v_a^{\text{Low}} - v_w^{\text{Low}}$ and $v_w^{\text{Upp}} - v_a^{\text{Low}}$. The SC energy Area III corresponds to the sum of $E_a^{\text{Low}} + E_a^{\text{Upp}}$ and the SC voltage Area III corresponds to the region $v_{\text{min}} - v_a^{\text{Low}}$ and $v_a^{\text{Upp}} - v_{\text{max}}$.

When $v_{\text{SC}} = v_{\text{SC}}^{\star}$ it means that the SC SoC is recovered, no RRL is performed, hence, $max[t]$ and $min[t]$ are set to 0. When v_{SC} starts to fluctuate between the values v_w^{Low} and v_w^{Upp} the RR limits are set to $max[t] = +r_n$ and $min[t] = -r_n$. Given the DSO/TSO RRL limit in % of nominal power per minute, RRL_{nom}, the value r_n in W/s is calculated by

$$r_n = RRL_{nom} \cdot P_{DRES}^{nom}/60 \tag{9}$$

where P_{DRES}^{nom} is the nominal power of the DRES. Hence, in Area I the RRL can be provided in its full form to the DSO/TSO. The SC energy absorbed for ramp-ups is E_n^{Upp} and the SC energy released for ramp-downs is E_n^{Low}. It is taken that $E_n^{\text{Upp}} = E_n^{\text{Low}}$ and both these SC energy regions correspond to Area I. Based on this, the SC voltage boundaries for Area I are determined as:

$$E_n^{\text{Low}} = 0.5 \cdot C \cdot \left[(v_{\text{SC}}^{\star})^2 - (v_w^{\text{Low}})^2\right] \tag{10}$$

$$E_n^{\text{Upp}} = 0.5 \cdot C \cdot \left[(v_w^{\text{Upp}})^2 - (v_{\text{SC}}^{\star})^2\right] \tag{11}$$

If v_{SC} lies within Area II (Warning Area) the RRL is deteriorated to a value equal to r_w, which is a function of the voltages difference until the alert area with boundary limit $r_a = \pm k \cdot |r_n|$. Note that the parameter $k > 1$ is a positive integer. In this area, the AS is partially provided for both ramp-ups (E_w^{Upp}) and ramp-downs (E_w^{Low}) with $E_w^{\text{Upp}} = E_w^{\text{Low}}$. As illustrated in Fig. 3, the voltage difference follows a linear approach $r_w(v)$. This approach have been especially suited to be implemented in the same microcontroller that performs the control of the VSC with execution time in the order of μs (here, $\Delta t = 50\mu s$). The linear approach is given by:

$$r_w^{\text{Upp}}(v) = r_n + r_n \cdot (k-1) \cdot \frac{v - v_w^{\text{Upp}}}{v_a^{\text{Upp}} - v_w^{\text{Upp}}} \tag{12}$$

$$r_w^{\text{Low}}(v) = -r_n + r_n \cdot (k-1) \cdot \frac{v - v_w^{\text{Low}}}{v_w^{\text{Low}} - v_a^{\text{Low}}} \tag{13}$$

In Area II the voltage boundaries are given by:

$$E_w^{\text{Low}} = 0.5 \cdot C \cdot \left[(v_w^{\text{Low}})^2 - (v_a^{\text{Low}})^2\right] \tag{14}$$

$$E_w^{\text{Upp}} = 0.5 \cdot C \cdot \left[(v_a^{\text{Upp}})^2 - (v_w^{\text{Upp}})^2\right] \tag{15}$$

If k is set equal to 1, this means that Area II does not exist, i.e., the AS is fully provided with r_n within the region $v_a^{\text{Low}} - v_a^{\text{Upp}}$.

In Area III (Alert Area) the AS is not provided at all, since the SC is close to its operational limits. The respective voltage limits are illustrated in Fig. 3.

III. Experimental Validation and Comparison

In this section the proposed RRL method is validated in a real experimental testbed and compared to the LPF and MA approaches.

A. System under Study

The studied topology is a real testbed in the laboratory of Universidad de Sevilla (USE) developed under the framework of the H2020 project EASY-RES, [25], and is illustrated in Fig. 4. Its main components are: (i) A 20 kVA three-phase three-wire VSC with V_{DC}^{rated}=750V and V_{AC}^{rated}=400V; (ii) A SC of 6 F and 160 V, [21], with maximum instantaneous power of $2kW$; It should be noted that the total SC energy is $21.33Wh$, however, due to the safety voltage limits recommended by the SC manufacturer ($v_{\text{min}} = 90V$), the total SC energy used for RRL control is equal to $9.33Wh$; (iii) A controllable DC current source. The proposed control algorithm has been implemented in a Texas Instruments TMS320F28335 Delfino microcontroller with a sampling frequency of 20 kHz.

Regarding the SC voltage areas, the parameters in Fig. 3 have been derived using (10), (11), (14) and (15) and following a bottom-up approach in order to respect the limits recommended by the SC manufacturer: (i) v_w^{Upp}=145V and v_a^{Upp}=150V. This leads to E_a^{Upp}=4,425kWs (1.23Wh); (ii) Considering v_w^{Upp} with $v_{\text{SC}}^{\star}$=130V leads to E_w^{Upp}=12,384kWs (3.44Wh); (iii) Considering $v_{\text{SC}}^{\star}$ and E_w^{Low}=12,384kWs=E_w^{Upp}, it is calculated v_w^{Low}=113.03V; (iv) Considering v_w^{Low} and E_a^{Low}=4,425kWs=E_a^{Upp}, it is calculated v_a^{Low}=106.3V. The remaining parameters of Fig. 4 can be found in [22].

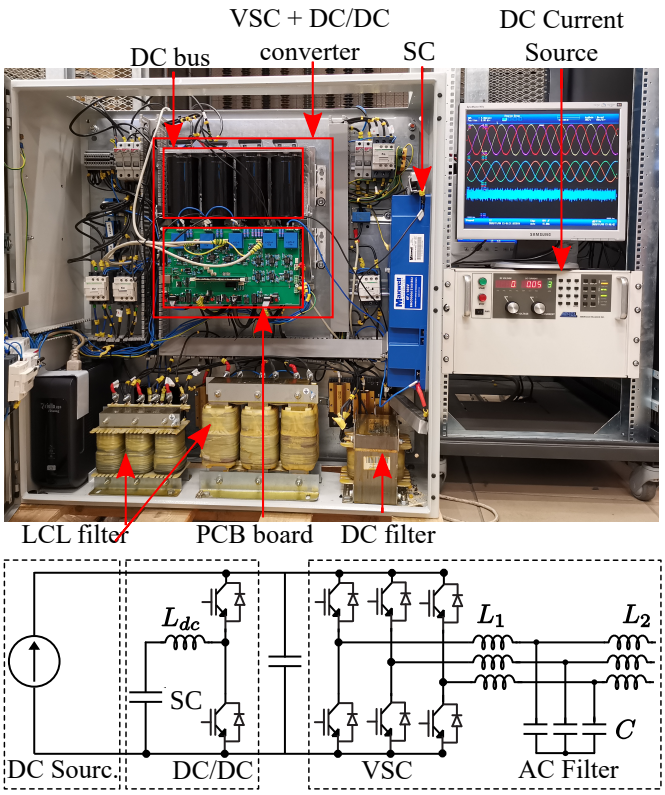

Fig. 4. Experimental Testbed with the detailed configuration

B. Evaluation of RRL Limit

The experimental validation aims to evaluate the efficiency of the RRL control and the effect of r_n. The data of the experimental results were recorded into the real-time platform SpeedGoat, which is suitable for recording data in steady-state conditions, since it communicates with the microcontroller and exchanges data (voltages, currents, etc.) every $0.5s$.

The input power signal p_{in} has been chosen to exhibit step-changes, as illustrated with the red curve in Fig. 5. The selected r_n values are 75, 100 and $150W/s$. Fig. 5(a) depicts p_{in} together with the output power of the algorithm p_{out}. Fig. 5(b) depicts p_s and p_{in}. The p_s is approximately $1kW$ less than p_{out} due to the power losses incurred on the lab testbed of Fig. 4. As it can be observed, the RRL control works perfectly and injects smoothed power to the grid. Moreover, the lower the r_n, the smoother is the active power p_{out} and p_s, as expected. This effect is very clear during ramp-ups ($0-50s$ and $150-200s$), because the SC does not reach its power or voltage limits, i.e.: (i) the SC power reaches barely its maximum power limit -$2kW$ (SC charging) in Fig. 5(c); (ii) the SC voltage does not reach 150V in Fig. 5(d).

During the successive ramp-downs (SC discharging) at time interval $50-150s$ both p_{out} and p_s are smoother than p_{in}, However, in cases where $r_n = 75$ and $100\ W/s$ the RRL is deteriorated according to (13) - especially during the 2^{nd} ramp-down, since the SC limits are reached: (i) the SC power instantaneously exceeds its maximum power limit 2kW (discharge) in Fig. 5(c); (ii) the SC voltage reaches its lower limit 106.3V in Fig. 5(d). The RRL method is evaluated with respect to the target RRL value considering as performance index the $RR(t)$ given in (8), [5], for $\Delta t = 1s$. This is

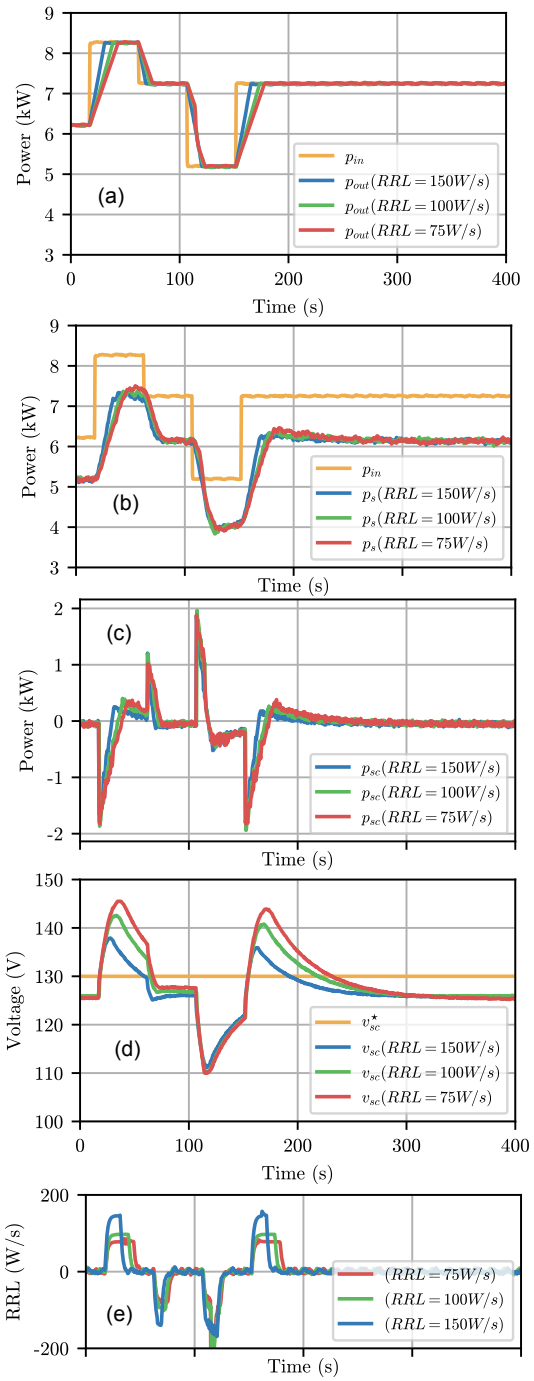

Fig. 5. Comparison of Different r_n values: (a): Input Power p_{in} and RRL output p_{out}; (b): p_{in} and resulting p_s to the grid; (c) SC power; (d) SC voltage; (e) Resulting RRL of the grid power p_s

reflected in Fig. 5(e), where the resulting RR in the grid power p_s is depicted. It can be observed very clearly that the target RRL value (r_n) is reached when the SC voltage stays within the predefined limits $E_a^{\text{Low}} - E_a^{\text{Upp}}$, i.e. 106.3-150V. Only in the time period $100-150s$ (2^{nd} ramp-down) the SC voltage limits are reached for the cases 75 and 100 W/s and thus, the target r_n value is not achieved. For $r_n = 150W/s$, the RRL is kept at its target value, since this value is not so strict and does not push the SC towards its limits.

Concluding this round of experiments, it can be deduced that the proposed RRL control is efficient and the target RRL values are well achieved respecting the safety limits of the

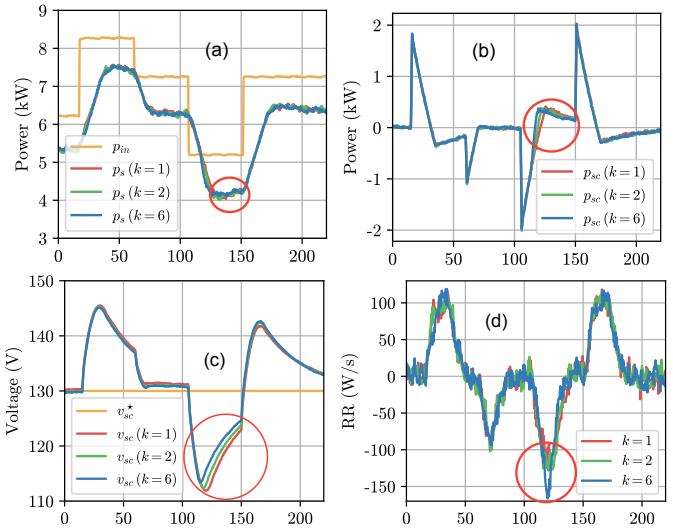

Fig. 6. Experimental Results - Evaluation of Warning Area with different k values: (a) Grid injected Active Power; (b) SC Power; (c) SC Voltage; (d) RR Calculated with (8).

SC. After the ramping events ($t > 200s$) the SC returns to its $v^{\star}_{\text{SC}}$ avoiding any oversmoothing and unnecessary operation. It should be mentioned that the studied target values of RRL $(75, 100, 150W/s)$ are too strict for the specific SC limits and size. Imposing a target RRL of $10 - 50W/s$ would destroy the specific SC. Larger size of SC could allow such low target values. This is evaluated in Section IV.

C. Evaluation of the Warning Area

In this subsection the effect of the Warning Area (Area II) is experimentally evaluated and more specifically, the effect of the parameter k in (12)-(13). The same step profile p_{in} has been used in the experiments. The target RRL is r_n=100W/s, while k is taken equal to 1, 2 and 6. The voltage limits are the ones set in Section III-A. The aggregated results appear in Fig. 6. The effect of the parameter k is very clear at the time interval $t = 120 - 150s$ and is marked with red circles in all subplots of Fig. 6. In all cases the grid injected power, p_s is very smoothed compared to p_{in} - Fig. 6(a) and the proposed control manages to pose the RRL of $\pm 100W/s$ in case $k = 1$, while in case $k = 2, 6$, the RRL $< 150W/s$ (absolute value). For k=1 the RRL control stresses the SC at $t = 120s$ and the SC voltage in Fig. 6(c) is below $113V$, i.e., below the Area II limit v_w^{Low}. Thus, the linear variation of (13) is activated for $k = 2, 6$. Increasing k leads the SC to operate in higher voltage values, hence in a safer region, while simultaneously keeping the RRL target below a certain pre-defined limit, which is defined continuously by (13) based on v_{SC}. As it can be noticed in Fig. 6(d) the achieved RRL is again below 150W/s and the RR is restricted to a specific value based on v_{SC} without exhausting the safety limits. It can be concluded that the introduction of the warning area in this RRL method ensures smoother p_s with a specific r_n and a safer SC operation for a given SC size.

D. Comparison with the LPF and MA approaches

In this subsection, the proposed RRL control is compared via experiments to a first order LPF, [5], [12], [19] and

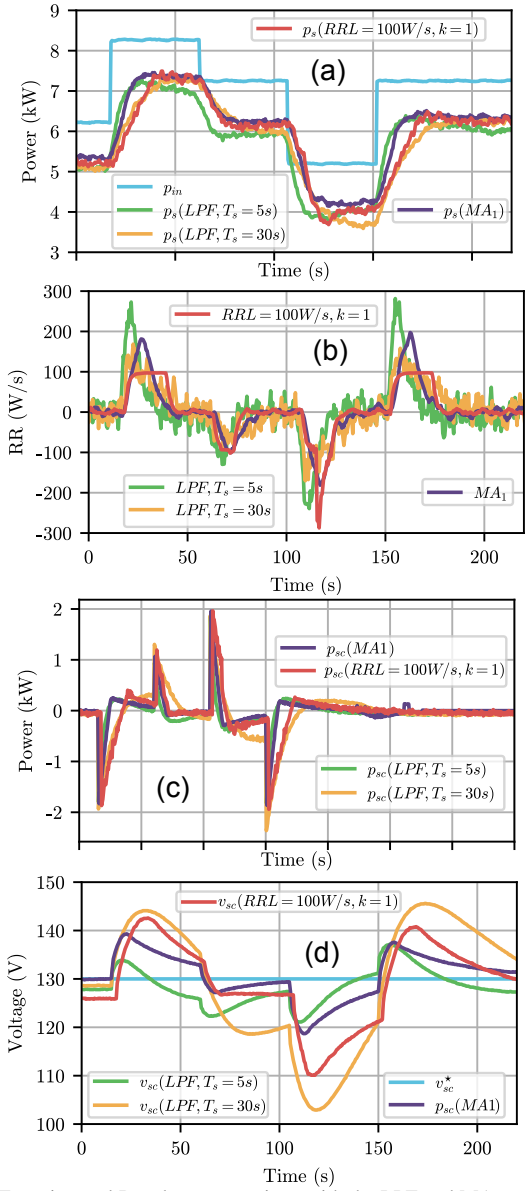

Fig. 7. Experimental Results - comparison with the LPF and MA approaches: (a) Grid injected Active Power; (b) RR Calculated with (8); (c) SC Power; (d) SC Voltage.

the sliding window MA method in terms of performance considering the same step profile as in the previous subsection. Generally, the first-order LPF has a transfer function in the continuous ($H(s)$), [12], and in the discrete ($H(z)$), [5], domain as:

$$H_{LPF} = \begin{cases} H(s) = \dfrac{1}{s \cdot T_{LPF} + 1} \\ H(z) = \dfrac{z^{-1}\left(T_s/T_{LPF}\right)}{z^{-1}\left(T_s/T_{LPF}\right) + 1} \end{cases} \tag{16}$$

where T_{LPF} is the time constant of the LPF and T_s is the sample time of the discretization. Several values for the T_{LPF} have been reported in the literature for different ESS types, e.g., $70s$ to $370s$ for a BESS in [5] and $600s$ for a SC in [12]. A very high T_{LPF} value stresses the SC due to continuous charging/discharging cycles in order to provide a smooth power at the DRES PCC -sometimes, smoother than actually required.

In the sliding window MA method, [5], [6] the previous active power DRES values are averaged for a given window of time, Δt_{w}. Depending on Δt_{w}, the power smoothing action will be more or less significant. The smoothed power is calculated:

$$p_{out}[t] = \frac{1}{N}\sum_{i=0}^{N} p_{\text{in}}[t - i \cdot \Delta t] \tag{17}$$

where N is the number of the samples that precede time instant t, forming a moving window with length equal to $\Delta t_{\text{w}} = N\Delta t$. Irrespectively of Δt_{w}, all samples have equal weight in the sliding window MA method. The reference signal sent to the SC is mathematically represented at a k^{th} instant by:

$$p^{\star}_{\text{SC}}[k] = \frac{\sum_{i=0}^{w-1} p_{\text{in}}[k-i]}{\Delta t_{\text{w}}} - p_{\text{in}}[k] \tag{18}$$

Similarly to the LPF approach, it can be derived that a very high the Δt_{w} of the sliding window MA method can stress the SC. Generally, it is known that usually BESS suffer from a small number of cycles (from $800 - 3,000$), while for SCs the number of cycles can vary from $200,000 - 500,000$, [27], [28]. However, the purchase cost of a BESS can vary from $400 - 600$€/kWh, while the SC (bank, not cell) capital cost is $\approx 20,000$€/kWh, [3], [28], [29]. Although the cost of BESS cycle/installed kWh can be up to 4 times larger than the SC, the SC cost per cycle and installed kWh is not negligible. Hence, it is yet important to evaluate the number of charging/discharging cycles, especially for AS like power smoothing at DRES level, where there are high fluctuations in the order of some seconds and the SC is continuously charged or discharged.

The target RRL is $r_n = 100W/s$ for the proposed control and there is no warning area for this round of experiments, i.e., $k = 1$. The LPF time constants that have been considered are $T_{LPF} = 5, 30s$. These values have been selected in order to respect the safety limits imposed by the SC manufacturer. For the sliding window MA approach Δt_{w} has been selected to be $4.95s$. The sampling rate of the data is $0.075s$, hence, the DSP of the CI-DRES topology needed to perform the MA around 99,000 samples, since the control is performed every $\Delta t = 50\mu s$. A larger Δt_{w} would result into more samples than the DSP can process and it would be overloaded. Note that the DSP is part of the CI-DRES of Fig. 4, which should be used for other AS as well, hence, the DSP should not be overloaded by only one AS, RRL in this case.

The results are depicted in Fig. 7. In Fig. 7 (a) it can be noticed that all approaches lead to smoother injected active power. The performance is further evaluated in Fig. 7 (b), where the RR is calculated based on (8). In all cases the RR is less than $300W/s$, however, only the proposed approach restricts the RR to a specific value $100W/s$ except for the time interval $t = 110 - 120s$ where the minimum SC voltage limit and the maximum SC power are reached -Fig. 7 (c) and (d). The LPF case $T_{LPF} = 5s$ always underperforms compared to the proposed approach and the achieved smoothing is not as efficient as with the proposed RRL method -Fig. 7 (b). For this reason, in this case the SC operates always in safer power (Fig. 7 (c)) and voltage areas (Fig. 7 (d)). Similarly, the $T_{LPF} = 30s$ case underperforms compared to the proposed approach during ramp-ups ($t = 20s$ and $t = 150s$), while for the rest of the

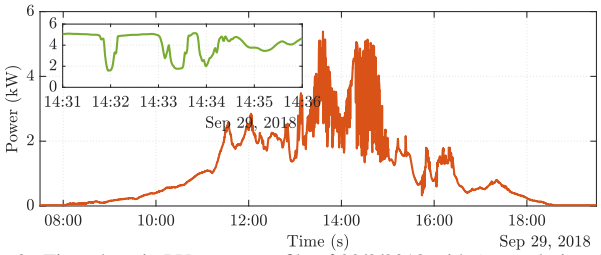

Fig. 8. Time-domain PV power profile of 29/9/2018 with $1s$ resolution, [15] - Zoom in the 300 seconds (14:31-14:36) used as input profile in the simulations

experiment duration it leads to a power "oversmooth" below the target r_n. As evident in Fig. 7 (c)-(d), this action leads the SC to operate closer to its safety limits, although it is not necessary: (i) during the 2^{nd} ramp-down ($t = 110 - 120s$) the SC reaches lower voltage (closer to the limit) than in the proposed approach; (ii) during the 2^{nd} ramp-up ($t = 150s$) the SC reaches higher voltage and lower power than in the proposed approach. The MA method with selected $\Delta t_{\text{w}} = 4.95$ does not exhibit large voltage fluctuations, however, the SC power limits are reached at $t = 20s$ and $t = 150s$ during ramp-ups and at $t = 60s$ during the ramp-down. During these ramp-ups the target $r_n = 100W/s$ cannot be achieved. The same is true for the ramp-down at $t = 120s$, although the SC voltage or power limits are not reached. This behavior is justified by the fact that with the MA approach the achieved RRL cannot be pre-evaluated.

Concluding this experimental round, it can be deduced that the proposed control reaches exactly the target RRL compared to the LPF and sliding window MA approaches, while respecting the SC safety limits. On the other hand, in the LPF and MA methods it is very difficult to pre-evaluate the achieved RRL. The LPF approach tends to oversmooth the power. This oversmoothing action leads to larger SC voltage oscillations, hence, deeper charging/discharging cycles, which deteriorate the SC life cycle. Further evaluation on the SC charging/discharging cycles is provided in Section IV. The selected window of the MA approach does not respect the selected RRL but this window cannot be increased, because it would lead to a DSP overloading.

IV. Simulation Results and Economic Evaluation

In this Section the proposed control and the complete lab topology of Fig. 4 is modelled in Matlab/Simulink so as to allow comparisons regarding different control parameters, SC sizes, and more fluctuating real-life profiles. The simulation results will provide a further insight on the economic aspects for the power smoothing provision as an AS.

A. Effect of Different Parameters

The effect of k and the SC size on the proposed RRL control are evaluated in this subsection. More specifically, k is set equal to 1 (no warning area) and 4, i.e. in the warning area there is linear variation $r_w(v)$ between 100-400W/s using (12)-(13). The SC sizes that have been considered are the real lab 6F/160V SC of [21] and the 8F/160V SC of [30] of the same manufacturer and with the same nominal voltage as [21]. The 8F/160V SC of [30] has been selected to be simulated and

compared to the real lab 6F/160V SC because both SCs are from the same manufacturer, have the same rated voltage and the same recommended safe operation region, $v_{\min} - v_{\max} = 90 - 150V$. Since these limits are the same, the voltage limits of Fig. 3 are also the same, and only the capacitance size is evaluated. In addition, simulations are performed in this section with a fictional SC of 4F/160V SC to demonstrate more clearly the effect of the C and k values. The involved energy areas of the 8F SC and 4F SC in Fig. 3 are increased by 2/6=33.33% and decreased by 33.33% respectively. The input signal p_{in} is a $300s$ profile with abrupt changes. These data have been isolated from the measured PV profile of Fig. 8 with $1s$ resolution, which corresponds to a $6.5kW_p$ PV PP in Germany (DSO data in [15]). This $300s$ profile has been selected over the whole day as a "worst-case" profile, because it presents the higher and most frequent RR values and the SC will suffer the most. This is considered as a typical Central European PV profile in a cloudy day. The target RRL value has been selected to be r_n=100W/s. The voltage limits are the ones set in the previous subsection.

The aggregated results appear in Fig. 9. The studied areas are marked with red ellipses. The following general observations can be made with respect to the efficacy of the algorithm: (i) In all cases the grid injected power, p_s is very smoothed compared to p_{in} - Fig. 9(a); (ii) It can be noticed in Fig. 9(b) that in all cases the SC reaches its upper and lower power limits at time instants $t = 150s$ and $t = 250s$, respectively. (iii) After very abrupt ramping events ($t > 300s$) the SC starts to return to its $v^{\star}_{\text{SC}}$, because the RR of $p_{in} < r_n$, avoiding in this way any oversmoothing and unnecessary operation.

The effect of parameters k and the SC size is very clear in the SC voltage - 9(c). At t=160s and for C=4F/k=1 the RRL control stresses the SC and it reaches its lower safety limit $v_{\min} = 90V$, hence the requested RRL cannot be achieved (yellow line). Introducing the warning area with $k = 4$ to the C=4F, the RRL is limited from 1000W/s to 400W/s (9(d)) and v_{SC} is higher than $v_{\min}$ leading the SC operation to a safer voltage region for this specific SC size. The ramp-down at $t = 240s$ leads also the SC to operate below 110V for $k = 1$ while for $k = 4$ the warning area is activated according to (13) leading the SC voltage to higher values, while the RRL is below 400W/s. However, this specific SC size is not appropriate for the ramp-up at t=260s; even when Area II is activated, the requested RRL cannot be achieved. Increasing the SC value to C=6F leads always the SC to operate within the safety limits recommended by the manufacturer. Nevertheless, for C=6F/k=1 the SC operates close to its lower safety limit at t=160s. Increasing k=4 leads the SC to operate in higher voltage values - a little bit closer to its upper voltage limits (at t=260s)- but generally, the RRL control leads the SC operation into a safer area, while simultaneously keeping the RRL below a certain pre-defined limit, i.e., $400W/s$. Compared to C=6F/k=1, increasing C to 8F achieves the same smoothing ($\pm 100W/s$) but this allows the SC to operate in a much more safer region (around 110-140V). For the case C=8F/k=4 the SC again operates around 110-140V leading to the conclusion that with higher C the warning area could be omitted and the RRL could have a lower

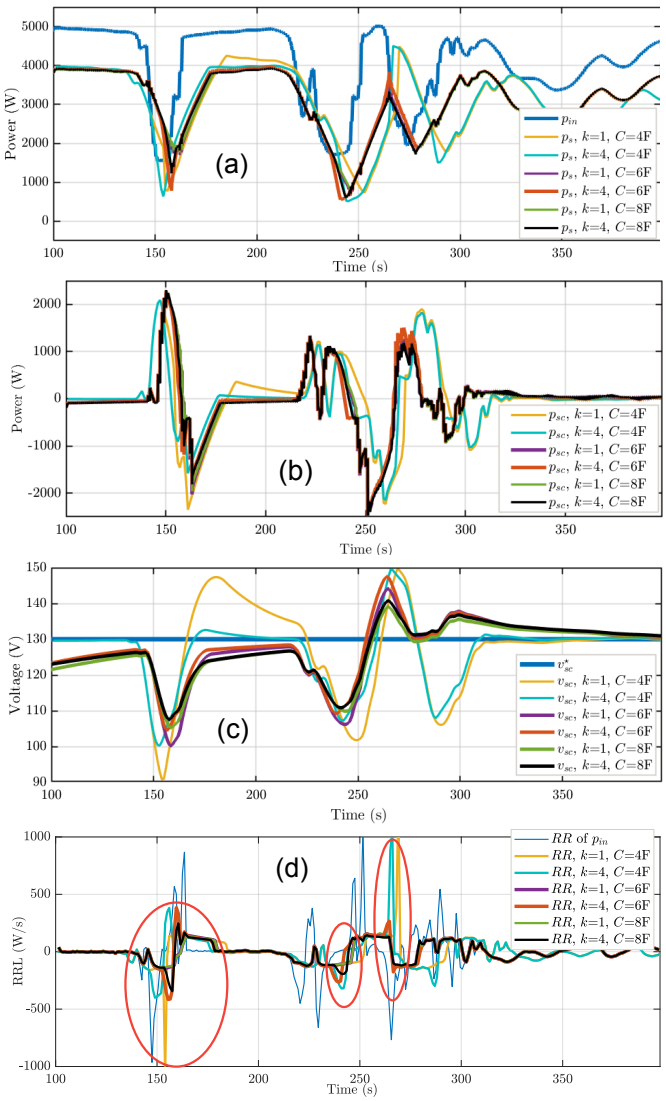

Fig. 9. Results for different values of k and SC size: (a) Grid injected Active Power, p_s and p_{in}; (b) SC Power; (c) SC Voltage; (d) RR computed by (8).

value (stricter RRL/better smoothing). Of course, increasing the SC size leads to better smoothing effect in p_s. However, larger sizes may lead to excessive ESS costs, as discussed in the following Sections. Hence, the introduction of the warning area can lead to reduced SC size. Finally, it can be concluded that the introduction of the warning area in this RRL method ensures smoother p_s with a specific r_n (or within a specific pre-defined range of r_n values) and with a safer SC operation for a given SC size compared to the case where other control approaches are applied and the SC size is not large enough and the power smoothing functionality is disabled when the SC reaches its limits . Such case could cause further undesired effects at power system level.

B. Comparison with the LPF and MA approaches

In this subsection, the proposed RRL control is compared via simulations to a first order LPF and the sliding window MA, in terms of performance and relative cost increase considering as p_{in} the $300s$ profile of Fig. 8. Both the LPF and MA control schemes are activated when the SC voltage is within the limits 90V-150V to respect the safety limits

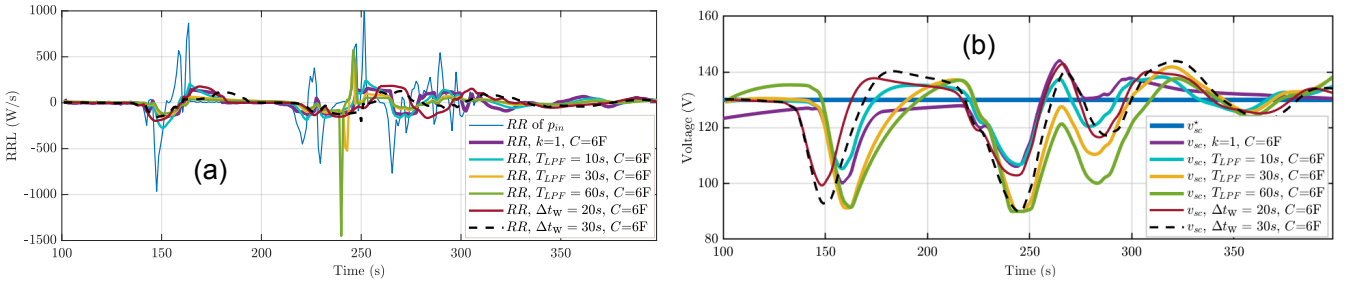

Fig. 10. Comparison among the proposed RRL approach, the LPF method and the sliding window MA method considering SC capacity $C = 6F$: (a) Achieved RR, W/s; (b) SC voltage.

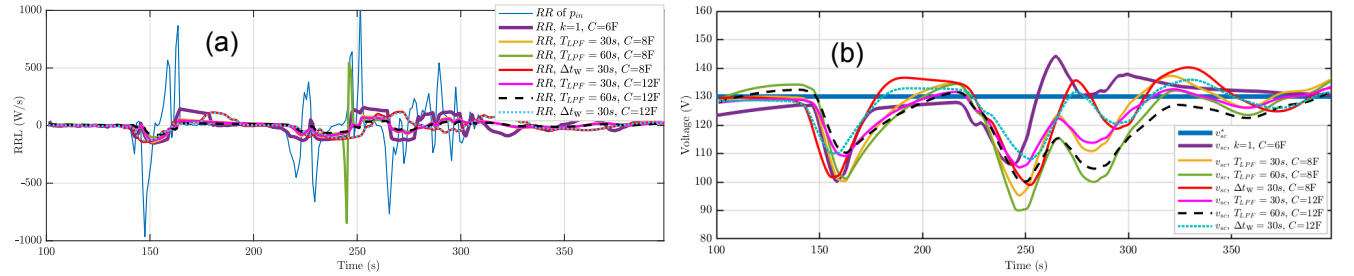

Fig. 11. Comparison among the proposed RRL approach, the LPF method and the sliding window MA method considering larger SC capacities for the LPF approach: (a) Achieved RR, W/s; (b) SC voltage.

imposed by the SC manufacturer. For the proposed method the selected case is the one with target RRL $100W/s$, $k = 1$ and $C = 6F$, as shown in Fig. 10(a)-(b). The selected T_{LPF} are 10, 30, and 60 s and the selected Δt_{w} are 20 and 30 s. Regarding the LPF method, none of the LPFs manages to keep the RR at specific limits: in the case of $T_{LPF} = 10s$, the achieved smoothing is not as efficient as with the proposed RRL method. This is evident in the successive ramp downs and ups in the time intervals $t = 140 - 170s$ and $t = 240 - 270s$. For $T_{LPF} = 30s$ and $T_{LPF} = 60s$ in most of the time an oversmoothing appears compared to the proposed RRL method. This oversmoothing leads to higher SC voltage fluctuations compared to the proposed approach, hence, deeper charging or discharging of the SC. At simulation time interval $t = 240s - 250s$ the smoothing action stops, since the SC reaches its lower voltage limits. Hence, the existing SC bank capacity of $6F$ is not adequate for the LPF control. Regarding the MA method, the selected Δt_{w} generally exceed the target RRL compared to the proposed approach, while leading to larger voltage fluctuations. This is an undesired effect since high SC voltage or SC power fluctuations actually reflect the depth of the charging/discharging cycles -an evaluation on the full charging/discharging cycles appears in the following subsection. Again the target RRL cannot be pre-evaluated.

In order to show the relative increase in the SC size, another round of simulations is performed. More specifically, the manufacturer voltage limits have been considered the same, while the capacitance is increased by 40% (C=8F) and 100% (C=12F). These results appear in Fig. 11. As it can be observed, when increasing the SC size, both the LPF and MA approaches manage to smooth efficiently the power (Fig. 11 (a)), except in the case of $T_{LPF} = 60s$ and $C = 8F$, where the voltage limits are reached at $t = 340s - 350s$ (Fig. 11 (b)). Based on the results of Fig. 11, it can be deduced that an increase in the SC size by 40% or 100% would lead to the respective increase of the SC price when operating with the LPF or the MA approach. Considering that the lab SC cost is $\approx$ 1000€, the additional cost for applying the LPF approach is 400 to 1000€ more than when applying the proposed approach. Moreover, the cost of the DC filter is 200€ and the cost of the associated DC/DC converter is 500€ (rated power $2kW$). If the power of the SC and the associated DC/DC converter need to be larger as well, further cost increase would be needed, leading to an increase larger than 50% when applying the LPF or the MA approach compared to the proposed RRL control.

C. Economic Evaluation

Economic comparisons for the ESS size are usually conducted in the literature considering "worst-case" scenarios from historical data (daily or yearly profiles), [12], [15], [17], [18]. In order to allow a more comprehensive economic comparison between the proposed RRL method and the LPF and the MA approaches, simulations with daily profiles need to be performed. As a "worst-case" daily profile, the PV daily profile of Fig. 8 has been used. To allow such comparisons, the detailed Simulink model used is the previous subsection is simplified to an analytical Matlab model, in a similar manner to [19]. The losses in the lab topology are ignored, i.e., $p_{\text{out}} = p_s$. For a given time instant the smoothed power is calculated by **Algorithm 1**. For the sliding window MA p_{out} is given by (17), while for the LPF, the smoothed power is derived by:

$$p_{\text{out}}[t] = \frac{2T_{LPF} - \Delta t}{2T_{LPF} + \Delta t} \cdot p_{\text{out}}[t - \Delta t] + \\ + \frac{\Delta t}{2T_{LPF} + \Delta t} \cdot (p_{\text{in}}[t] + p_{\text{in}}[t - \Delta t]) \quad (19)$$

In this investigation, for the proposed approach, the target values of r_n are 32.5, 75, 100 and 150 W/s and there is no warning area, i.e., $k = 1$. Different values of T_{LPF} and Δt_{w} have been applied to (17) and (19), respectively. Considering an average cost of 1000€/kW_p for the PVPP,

TABLE I
RESULTING SC POWER, ENERGY AND COST FOR ONE DAY SIMULATIONS

Method	**Power**, W	**Energy**, Wh	$RR_{out}^{max}, W/s$	**RC** %
r_n =32.5 W/s	2,875	586.7	32.5	180.5
r_n =75 W/s	2,597	302	75	92.9
r_n =100 W/s	2,448	219.4	100	67.5
r_n =150 W/s	2,173	123.6	150	38
$T_{LPF} = 5s$	2,017	326	340	100.3
$T_{LPF} = 15s$	2,616	678.5	166	208.8
$T_{LPF} = 30s$	2,776	972.6	91.68	299.3
$T_{LPF} = 81s$	2,673	1,445	32.67	444.6
$\Delta t_{\text{w}} = 20s$	2,644	598.03	168.94	184
$\Delta t_{\text{w}} = 30s$	2,877	781.52	117.96	240
$\Delta t_{\text{w}} = 60s$	3,204	1,155.17	61.34	355
$\Delta t_{\text{w}} = 100s$	2,818	1,371.7	35.87	422

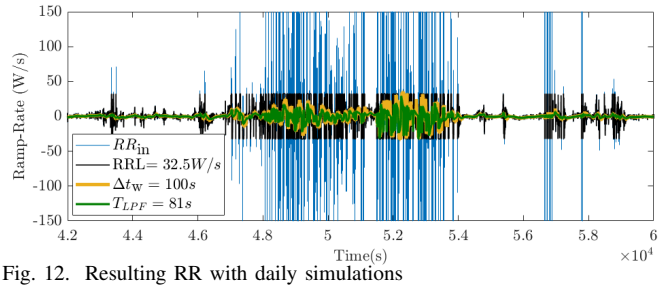

Fig. 12. Resulting RR with daily simulations

a 6.5 kW_p PVPP would cost 6,500€. Assuming an average SC cost of 20€/Wh, [3], the relative additional purchase cost of the SC with respect to the total PVPP cost is calculated and shown in Table I - denoted as **RC** (Relative Cost). The achieved RR in W/s is also shown in Table I. For the LPF and MA approaches, the RR of p_{out} cannot be pre-evaluated, hence, for the different values of T_{LPF} and Δt_{w}, the RR_{out}^{max} (maximum RR of p_{out} after applying the LPF or MA approach) is also shown in Table I. As it can be deduced, the proposed RRL results into much smaller SC size in terms of energy, while the maximum instantaneous power needed does not have important differentiation. For almost the same resulting $RR_{out}^{max} \approx 32.5W/s$, $RR_{out}^{max} \approx 100W/s$ and $RR_{out}^{max} \approx 150W/s$, the $T_{LPF} = 81s$, $T_{LPF} = 30s$ the $T_{LPF} = 15s$, $\Delta t_{\text{w}} = 20s$, $\Delta t_{\text{w}} = 30s$, $\Delta t_{\text{w}} = 60s$ and $\Delta t_{\text{w}} = 100s$ require almost 3-5 times larger SC energy than in the case of the proposed RRL with $r_n = 32.5W/s$, $r_n = 100W/s$ and $r_n = 150W/s$. In Fig. 12 the RR of the cloudy day profile is calculated by (8) and illustrated with blue line for the time interval 40,000-60,000s, i.e., 11:06:40-16:40:00 o'clock. The daily profile results for $T_{LPF} = 81s$, $\Delta t_{\text{w}} = 100s$ and $r_n = 100W/s$ are illustrated in Fig. 12, where the oversmoothing effect of the LPF and MA approaches is also evident.

Closing this round of investigations, it can be concluded that the proposed RRL control utilizes the least ESS capacity - hence, lower cost - than filter-based and MA methods, because the RRL control limits the RRL to a pre-determined specific level and allows the SC only to operate for significant fluctuations, thus, avoiding oversmoothing. Moreover, with the proposed approach the RRL can be pre-defined by the DSOs or TSOs. On the contrary, with the filter-based and MA approaches there is NO correlation of the filter time constant with the achieved RRL.

PREPA proposed RRL_{nom}=10%/min for the RRL to protect the system from significant RRs caused by non-dispatchable DRES, [2]. Currently, the most frequent approach, [12], [17], [18], is to size the ESS considering the worst case scenario, i.e. for (i) RRL=10%/min, which is the PREPA limit and it is considered very strict; (ii) $\Delta P = 0.9p.u$ with respect to the maximum DRES power within 10 minutes, [12] -which is a really high time interval for the SC, since it is a fast acting ESS. These sizing approaches usually do not consider the ESS cost. For example in [12] an SC of 1kWh is simulated considering a PV PP of 15kW_p without taking into account the associated cost involved. In this paper, the SC used energy is 9.3Wh and this specific SC size [21] in the lab was selected so as to cost around 10% of the total purchase and installation price of a 10kW_p PV PP. The relative additional purchase cost of the SC and the associated DC/DC converter must be considered if the SCs are needed to support the electric power systems with the provision of AS. Although there are plenty of studies taking into account the ESS cost for power smoothing (probabilistic, [31], search-based [32], etc., [15]) all of them consider for both DSs and TSs a RRL=10%/min without examining if such strict RR limits are suitable for DSs, where the effect of the loads may eliminate fluctuations caused by the DRES.

The RRL action should be evaluated **simultaneously** at DRES and power system level together with its impact on the power system stability. However, a step that should precede is the following: it should be ensured that this AS is provided with a relatively low additional cost with respect to the total DRES installation cost. In this section, an incremental (with respect to the current conditions) relative additional cost limit, **RC** of the SC and the associated DC/DC converter is imposed for offering RRL as an AS: **RC**$\leq$ 10%. The DRES that are taken into account have nominal power $P_{\text{DRES}}^{\text{nom}} < 100kVA$, [3]. The following assumptions are made: (i) cloudy day profile of Fig. 8; (ii) $RRL_{nom} = 0.3pu/min$, i.e., $r_n = 32.5W/s$ computed with by (9) and $k = 1$, i.e., no warning Area; (iii) For the LPF and MA methods, the value and $T_{LPF} = 81s$ and $\Delta t_{\text{w}} = 100s$ have been selected so as to achieve a similar RR_{out}^{max} as shown in the previous investigation. Moreover, $T_{LPF} = 30s$ and $\Delta t_{\text{w}} = 30s$ have been selected to demonstrate how the proper choice of these parameters affects the number of RRL violations and the SC charging/discharging cycles; (iv) the aforementioned unit costs of PVPP and SC, hence, total PVPP cost of 6,500€. This cost limit, RC=10% can be translated into SC energy limit: the SC should cost 650€ and considering the SC unit cost of 20€/Wh, the resulting SC energy is calculated to be 32.5Wh. Assuming that the SC should absorb and inject active power and that it should return to a specific SoC, it is required that the lower "instantaneous" energy limit is -16.25Wh and the upper "instantaneous energy" limit +16.25Wh. Since the SC should mitigate both ramp-ups and ramps downs, the SC should return to 50% SoC. Another parameter that is inserted in these simulations is the SoC recovery time. The SC recovery time is assumed to range between 0 to 3 minutes. When inserting those two parameters, violations in the RRL control will be met. The number of the "instantaneous" violations should be counted, since they affect the efficacy of the RRL provision.

The results are shown in Table II. For the examined cases the following can be deduced: (i) increasing the SC recovery time

TABLE II
COMPARISON - NUMBER OF VIOLATIONS OF THE RRL/r_n VALUE FOR SPECIFIC SC ENERGY AND RECOVERY TIME (s)

Recovery Time	**RRL,** $k=1$	$T_{LPF}=81s$	$T_{LPF}=30s$	$\Delta t_{\mathrm{w}}=30s$	$\Delta t_{\mathrm{w}}=100s$
0	24	101	722	1316	182
5	63	161	736	1330	208
10	99	215	742	1375	246
30	221	351	801	1391	371
60	302	593	825	1403	651
120	546	830	1013	1425	833
180	697	1131	1185	1547	1077

TABLE III
COMPARISON - NUMBER OF FULL CHARGE/DISCHARGE CYCLES FOR SPECIFIC SC ENERGY AND RECOVERY TIME (s)

Recovery Time	**RRL,** $k=1$	$T_{LPF}=81s$	$T_{LPF}=30s$	$\Delta t_{\mathrm{w}}=30s$	$\Delta t_{\mathrm{w}}=100s$
0	8/14	30/28	18/19	15/11	26/30
5	9/13	30/27	18/18	15/11	26/27
10	9/12	29/27	17/19	14/12	27/25
30	7/12	24/25	17/17	13/11	29/27
60	6/10	21/24	15/14	8/14	22/20
120	3/9	20/17	11/14	6/13	17/16
180	2/9	16/18	8/13	6/10	10/18

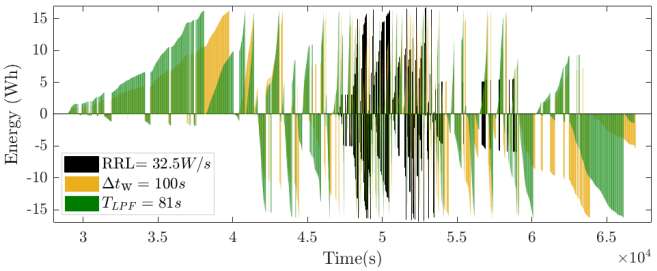

Fig. 13. Resulting SC charging/discharging cycles with daily simulations considering a recovery time of $30s$

leads to larger number of violations. However, the SC is a fast acting ESS and if appropriate SoC recovery control schemes, like [22], are applied, the SoC can recover in less than 60 s. This means that the proposed RRL control would have up to 300 violations. Considering around 12 hours (43,200 s) of solar irradiation within a day, this number is $< 0.7\%$. On the contrary, for $T_{LPF} = 81s$ and $\Delta t_{\mathrm{w}} = 100s$, this number can be 2-7 times larger. For $T_{LPF} = 30s$ it can be deduced that even if the SC SoC recovers in less than $30s$, the RRL violations can be 4-20 times more than the proposed approach and 3-7 times larger than $T_{LPF} = 81s$. For $\Delta t_{\mathrm{w}} = 30s$ it can be observed that even if the SoC is assumed to recover immediately, the RRL violations can be 3-55 times more than the proposed approach and 2-7 times larger than $\Delta t_{\mathrm{w}} = 100s$; (ii) for a specific SC energy capacity, between the three approaches, the most efficient one is the proposed method, since it leads always to fewer violations of RRL_{nom}.

With respect to the same cases, the number of full charging/discharging cycles have been estimated and the results are shown in Table III. The term "full charging/discharging cycle" corresponds to the case where the upper/lower SoC limit is reached, respectively. In Fig. 13 all charging/discharging cycles are depicted for recovery time equal to $30s$ considering all three approaches. It can be observed that there can be more charging/discharging cycles, but not full ones, since the successive ramp-ups and downs do not always exhaust the SC SoC limits. For all these cases the following can be deduced: (i) evidently, increasing the SC recovery time leads to smaller number of charging/discharging cycles; (ii) The proposed approach leads always to smaller number of cycles, even when $k = 1$, i.e., the target RRL value is always achieved; Regarding $T_{LPF} = 81s$ and $\Delta t_{\mathrm{w}} = 100s$, which respect the RRL target, it can be derived that the number of cycles is 2-7 times larger than the proposed approach. These methods have more cycles due to the fact that they tend to oversmooth the power (also evident in Figs. 12 and 13); (iii) decreasing the T_{LPF} or Δt_{w} can lead to reduction of the cycles, but at the cost that the desired smoothing is not achieved.

This final round of investigations proves that the RRL functionality can be performed meeting **simultaneously** RRL_{nom} and a specific limit in the **RC**. The cost limit impact on the provision of the RRL as an AS is important, if this AS is to be allocated to DRES owners as a mandatory system support function, in a similar manner to reactive power provision, or other AS, [3]. A design engineer can select a SC and the associated DC/DC converter based on the cost and then, evaluate if it can meet the required RRL using a representative daily profile. Finally, it should be noted that in all the cases examined in Tables I, II and III, the instantaneous power of the SC and its DC/DC converter is calculated to be $< 50\% P^{nom}_{DRES}$.

V. DISCUSSION & CONCLUSIONS

The RRL has been identified as a new AS to be provided by large-scale DRES connected directly at TS level. The RRL could serve as a proactive action towards the conventional unit commitment for frequency reserves. However, even in the weak TSs the use of BESS together with a PVPP has been proven to be ineffective in terms of performance due to the BESS slow dynamics. In this paper, a novel RRL control method has been developed to mitigate active power fluctuations at DRES level. The RRL function is performed by a SC, which is a fast acting ESS. The RRL control is simple enough to be implemented in the microcontroller of a real DRES and it can be directly applicable to any grid code requirements for RR limitation. Another advantage of this method is that the SC voltage (i.e. SoC) is taken into account *a-priori*, i.e. before the service is provided. For this reason, specific RRL can be ensured at the DRES connection point, without exhausting the ESS safety limits. Hence, the problem of oversmoothing and decreased operational life can be avoided. The RRL control itself does not have any

implementation restrictions, as long as suitable voltage limits and realistic RRL target values (with respect to a specific SC size) are set. The effectiveness of the proposed scheme against a filter-based method and a moving average method is validated via experiments considering different values of RRL providing additional experimental contribution of this paper. The effect of the SC size and the RRL deterioration when the SC limits are reached are also investigated via simulations. In addition, the proposed approach is compared to a filter-based and a moving average method in a techno-economic manner considering several parameters, e.g., the SC recovery time, the SC size and cost. The proposed approach leads to 1.5-5 times smaller SC size compared to the other methods. In addition, when considering a specific SC size, and depending on various time frames of SC SoC recovery, the proposed approach presents 2-7 times fewer charging/discharging cycles prolonging the SC life and 2 times fewer RRL violations. Such analysis does not exist for SCs in the current literature.

The SCs are conventionally sized based on the "worst-case" fluctuation model and RRL $10\%/min$ without examining if such value is suitable for DRES placed within DS. In further future studies, the appropriate value of the target RRL value will be studied for PPs that are equipped with SCs and connected within DSs, so that a whole DS could provide RRL to the upstream TS as an AS and as a preventive action towards frequency disturbances, i.e., so as to improve the TS stability - a topic yet unexploited in the technical literature. In this way, the RRL can be treated as an AS in a decentralized manner, which may lead to deferral of investments at DS and TS level and the engagement and remuneration of both small DRES owners together with large-scale ESS operators.

Author Contribution

Kyriaki-Nefeli Malamaki (K.-N.M.) has performed the literature review in the current state-of-the-art (Section I). K.-N. M. and Francisco Casado Machado (F.C.M) have formulated the idea and the mathematical background (Section II). K.-N.M. has performed simulations in Matlab/Simulink to study the effect of various parameters (Section III and IV) and to compare the proposed method against state-of-the-art approaches. Andrei Mihai Gross (A.M.G.), and Georgios Kryonidis (G.K.) have performed simulations in C code to introduce the model in the experimental set-up (Section III). The experimental validation has been carried out by Manuel Barragan Villarejo, and A.M.G. (Section III). Also, K.-N.M., F.C.M. and G.K. have edited the figures. Jose Luis Martinez Ramos and Charis Demoulias have supervised this paper and reviewed the manuscripts.

Acknowledgments

This research is funded by the European Union under the Horizon 2020 project EASY-RES (GA 764090) and CERVERA Research Programme of CDTI, the Industrial & Technological Development Centre of Spain, under the Project HySGrid+(CER-20191019). The authors would like to thank Enrique Antonio Rodríguez-Gonzalez from University of Seville, Spain, for his valuable contribution in helping in the experimental validation during the revision of this paper.

References

[1] K.-N. Malamaki *et al*, "Ramp-Rate Control of DRES employing Supercapacitors in Distribution Systems," in *2021 International Conference on Smart Energy Systems and Technologies (SEST)*, pp. 1–6, 2021.

[2] K.-N. Malamaki *et al*, "D1.1 Description of the Metrics developed for the Quasi-Steady-State Operation and Report on the Review of the respective Current Grid Codes," *H2020 EASY-RES Project Deliv.*, 2018.

[3] C. S. Demoulias *et al*, "Ancillary services offered by distributed renewable energy sources at the distribution grid level: An attempt at proper definition and quantification," *Appl. Sci.*, vol. 10, no. 20, 2020.

[4] V. Gevorgian, M. Baggu, and D. Ton, "Interconnection Requirements for Renewable Generation and Energy Storage in Island Systems: Puerto Rico Example," in 4^{th} *International Hybrid Power Systems Workshop, Crete, Greece*, May 22–23 2019.

[5] J. Martins, S. Spataru, D. Sera, D.-I. Stroe, and A. Lashab, "Comparative study of ramp-rate control algorithms for pv with energy storage systems," *Energies*, vol. 12, no. 7, 2019.

[6] J. Johnson *et al*, "Pv output smoothing using a battery and natural gas engine-generator," in *2013 IEEE 39th Photovoltaic Specialists Conference (PVSC)*, pp. 1811–1816, 2013.

[7] H. Liu, J. Peng, Q. Zang, and K. Yang, "Control strategy of energy storage for smoothing photovoltaic power fluctuations," *IFAC-PapersOnLine*, vol. 48, no. 28, pp. 162 – 165, 2015.

[8] M. J. E. Alam, K. M. Muttaqi, and D. Sutanto, "A novel approach for ramp-rate control of solar pv using energy storage to mitigate output fluctuations caused by cloud passing," *IEEE Trans. Energy Convers.*, vol. 29, no. 2, pp. 507–518, 2014.

[9] V. T. Tran, M. R. Islam, D. Sutanto, and K. M. Muttaqi, "Mitigation of Solar PV Intermittency Using Ramp-Rate Control of Energy Buffer Unit," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 435–445, 2019.

[10] A. Addisu, L. George, P. Courbin, and V. Sciandra, "Smoothing of renewable energy generation using gaussian-based method with power constraints," *Energy Procedia*, vol. 134, pp. 171 – 180, Jan. 2017.

[11] Ming Pang, Yikai Shi, W. Wang, and Xiaoqing Yuan, "A method for optimal sizing hybrid energy storage system for smoothing fluctuations of wind power," in *2016 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, pp. 2390–2393, 2016.

[12] L. G. González, R. Chacon, B. Delgado, D. Benavides, and J. Espinoza, "Study of energy compensation techniques in photovoltaic solar systems with the use of supercapacitors in low-voltage networks," *Energies*, vol. 13, no. 15, 2020.

[13] J. F. Patarroyo-Montenegro, J. D. Vasquez-Plaza, O. F. Rodriguez-Martinez, Y. V. Garcia, and F. Andrade, "Comparative and Cost Analysis of a Novel Predictive Power Ramp Rate Control Method: A Case Study in a PV Power Plant in Puerto Rico," *Appl. Sci.*, vol. 11, no. 13, 2021.

[14] Y. S. Perdana, S. M. Muyeen, A. Al-Durra, H. K. Morales-Paredes, and M. G. Simões, "Direct Connection of Supercapacitor–Battery Hybrid Storage System to the Grid-Tied Photovoltaic System," *IEEE Trans. Sustainable Energy*, vol. 10, no. 3, pp. 1370–1379, 2019.

[15] Malamaki, K.-N. *et al*, "D1.3 1st report on the reactive power control algorithm for converter-interfaced dres/bess and analytical tool for parametric bess sizing for low-frequency power smoothing," *H2020 EASY-RES Project Deliv.*, 2019.

[16] S. Sukumar, M. Marsadek, K. Agileswari, and H. Mokhlis, "Ramp-rate control smoothing methods to control output power fluctuations from solar photovoltaic (pv) sources—a review," *Journal of Energy Storage*, vol. 20, pp. 218 – 229, 2018.

[17] J. Marcos, O. Storkël, L. Marroyo, M. Garcia, and E. Lorenzo, "Storage requirements for pv power ramp-rate control," *Solar Energy*, vol. 99, pp. 28 – 35, 2014.

[18] J. Marcos, I. de la Parra, M. García, L. Marroyo, "Control strategies to smooth short-term power fluctuations in large photovoltaic plants using battery storage systems," *Energies*, vol. 7, no. 10, pp. 6593–6619, 2014.

[19] G. C. Kryonidis, A. I. Nousdilis, K. D. Pippi, and T. A. Papadopoulos, "Impact of Power Smoothing Techniques on the Long-Term Performance of Battery Energy Storage Systems," in *2021 56th International Universities Power Engineering Conference (UPEC)*, pp. 1–6, 2021.

[20] S. D. Tragianni, K. O. Oureilidis, and C. S. Demoulias, "Supercapacitor sizing based on comparative study of PV power smoothing methods," in *2017 52nd International Universities Power Engineering Conference (UPEC)*, pp. 1–6, 2017.

[21] Maxwell Technologies, "160V - BMOD0006 E160 C02 Data Sheet, Wind Pitch Control Energy Storage 160V - 6F Module." Available [Online]:https://www.maxwell.com/products/ultracapacitors/downloads.

[22] A. Mihai Gross *et al*, "Energy Management In Converter-Interfaced Renewable Energy Sources Through Ultracapacitors For Provision Of Ancillary Services," in *2021 International Conference on Smart Energy Systems and Technologies (SEST)*, pp. 1–6, 2021.
[23] F. J. Matas-Díaz *et al*, "DC-bus energy management of a converter-interfaced renewable energy source comprising an energy storage system," in *2021 IEEE Madrid PowerTech*, pp. 1–6, 2021.
[24] EASY-RES Project, Funded by EU in the Frame of H2020 (GA:764090). www.easyres-project.eu.
[25] J. M. Maza-Ortega *et al*, "D6.1 Report Detailing the Implementation of Converter Prototypes," *H2020 EASY-RES Project Deliv.*, 2020.
[26] M. Ceraolo, G. Lutzemberger, D. Poli, "State-of-charge evaluation of supercapacitors," *Journal of Energy Storage*, vol. 11, pp. 211–218, 2017.
[27] A. G. Olabi, Q. Abbas, A. Al Makky and M. A. Abdelkareem, "Supercapacitors as next generation energy storage devices: Properties and applications," *Energy*, vol. 248, p. 123617, 2022.
[28] K. Mongird, V. Viswanathan, P. Balducci, J. Alam, V. Fotedar, V. Koritarov, and B. Hadjerioua, "An Evaluation of Energy Storage Cost and Performance Characteristics," *Energies*, vol. 13, no. 13, 2020.
[29] K. Mongird, V. Viswanathan, P. Balducci, J. Alam, V. Fotedar, V. Koritarov, and B. Hadjerioua, "Energy Storage Technology and Cost Characterization Report." Available [Online]: https://www.pnnl.gov/publications/energy-storage-technology-and-cost-characterization-report, PNNL-28866. Richland, WA: Pacific Northwest National Laboratory, 2019.
[30] Maxwell Technologies, "160V - BMOD0008 E160 B02 Data Sheet, Wind Pitch Control Energy Storage 160V - 8F Module." Available [Online]:https://www.maxwell.com/products/ultracapacitors/downloads.
[31] X. Wang, M. Yue, E. Muljadi, and W. Gao, "Probabilistic approach for power capacity specification of wind energy storage systems," *IEEE Trans. Industry Applications*, vol. 50, no. 2, pp. 1215–1224, 2014.
[32] Y. Yuan, C. Sun, M. Li, S. S. Choi, and Q. Li, "Determination of optimal supercapacitor-lead-acid battery energy storage capacity for smoothing wind power using empirical mode decomposition and neural network," *Electric Power Systems Research*, vol. 127, pp. 323 – 331, 2015.