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A Comprehensive Model of Step Voltage Regulators with Variable Taps in the Z-Bus Power Flow

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***Abstract*—This paper presents a comprehensive three-bus equivalent circuit model of three-phase step voltage regulators. The proposed model can accurately simulate any configuration of step voltage regulators and can be efficiently integrated in the Z-bus power flow method. Its distinct feature is that the taps are simulated outside the Y_{BUS} matrix in the form of current sources. As a result, the re-factorization of the Y_{BUS} matrix is avoided after every tap change reducing significantly the computational burden of the power flow analysis. Furthermore, possible convergence issues caused by the low impedance of step voltage regulators are addressed by introducing fictitious impedances, without, however, affecting the accuracy of the model. The proposed step voltage regulator model is validated in the IEEE 4-Bus and an 8-Bus network, while its performance is further investigated in the IEEE 8500-Node test feeder.**

***Index Terms*—Autotransformer, compensation technique, implicit Z_{BUS} power flow, step voltage regulator, tap variations, Y_{BUS} matrix factorization.**

1. Introduction

STEP voltage regulators (SVRs) are widely applied to low- (LV) and medium-voltage (MV) distribution networks to maintain voltages within permissible limits. They consist of autotransformers with adjustable turn ratios connected in several configurations e.g open-delta, close-delta, wye [1].

1.1 Literature Review on the steady-state SVR modeling

Only a few models have been proposed in the literature so far for the mathematical integration of SVRs into the power flow [1]-[4]. More specifically, the authors in [2] and [3] propose a mathematical formulation relating the primary and secondary voltages and currents, which is solved using the backward/forward sweep (BFS) method. In [4], a mathematical model of SVR is proposed, which is directly integrated in the Jacobian matrix, while the power flow is solved using the Newton-Raphson (NR) method.

However, these approaches are not applicable to the Z-Bus power flow since the SVR equations of [2]-[4] are not compatible with the formation of $\boldsymbol{Y_{BUS}}$ matrix. The Z-Bus power flow approach is a fixed-point iterative method, which is widely applied in distribution network applications, due to its high robustness, fast convergence, ease of implementation and low computation time [5]-[9]. Therefore, accurate and computationally efficient modelling of SVRs is significant in order for the Z-Bus method to maintain its superior characteristics.

Considering the integration of SVR models in the three-phase implicit Z-Bus power flow, a limited number of solutions has been proposed in the literature. A comprehensive SVR model is proposed in [1], which is applicable in all SVR configurations, while an open-delta SVR model is proposed in [10]. Although the aforementioned models are applicable in the Z-Bus power flow approach, the tap variables of SVR are simulated in the $\boldsymbol{Y_{BUS}}$ matrix of the network. As a result, a re-factorization (or inversion) of the Y_{BUS} matrix is required after every tap variation, thus increasing significantly the overall computational burden.

1.2 Challenges of efficiently modeling SVRs in the Z-Bus power flow

Ideally, the tap variables of the SVRs should be simulated outside the Y_{BUS} matrix of the network so that the re-factorization of the Y_{BUS} matrix is performed offline, only once, accelerating the power flow calculation. The compensation technique is usually implemented in the Z_{BUS} power flow to avoid the re-factorization of the $\boldsymbol{Y_{BUS}}$ matrix every time that one or more elements change [11]. According to this technique, the variable elements are modeled as fictitious current sources outside the $\boldsymbol{Y_{BUS}}$ matrix, thus the $\boldsymbol{Y_{BUS}}$ matrix remains always constant.

The compensation technique is applied in [7] and [11] to simulate transformers equipped with on-load tap changer (OLTC) in balanced networks (using single-phase power flow) and by the authors in [12] to simulate three-phase OLTC transformers in Y_g-Y_g configuration. However, in case of the SVRs, the implementation of the compensation technique results in the divergence of the power flow, due to the small impedance of SVRs, which in turn increases unacceptably the fictitious current sources. Similar conclusions about the divergence issues associated with the modeling of SVRs are derived in [13].

1.3 Technical contribution of this paper

This paper proposes a novel model, which overcomes the aforementioned divergence issues. The proposed model consists of a 3-bus equivalent circuit, which presents the following distinct characteristics:

- It simulates the taps of SVR as fictitious current sources outside the $\boldsymbol{Y_{BUS}}$ matrix, thus avoiding its continuous re-factorization after every tap variation. As a result, several real-time distribution management system (DMS) applications that require sequential tap variations are accelerated. Simulations conducted in the IEEE 8500-node network indicate that the proposed SVR model can reduce considerably the computation time of the power flow compared with the SVR model of [1].
- It is generic and can be applied in all SVR configurations i.e., wye, open-delta, closed-delta and types of SVRs i.e., Type A and Type B.
- The proposed model presents accurate power flow results since the applied equations are derived considering the exact three-phase SVR circuit. Simulation results confirm that the proposed model outputs identical power flow results with OpenDSS, Simulink and the model of [1], but with a significantly lower computation time.
- Although the taps are simulated in the form of current sources, the convergence of power flow is not compromised. Simulation results of the IEEE 8500-node network indicate that the proposed SVR model presents fast convergence speed.

1.4 Applicability of the proposed model

The DMS is a collection of applications designed to monitor and control the entire distribution network efficiently and reliably. A modern DMS includes several real-time optimization applications such as Volt/Var control (VVC) [20] [21], optimal feeder reconfiguration (OFR) and optimal power flow (OPF) [7]. More specifically, as soon as an estimate of the system load is obtained, DMS optimization functions compute new switching states of the local voltage controllers (e.g SVRs, OLTCs, capacitor banks, distributed generators) to optimize the system performance. The real-time power flow serves as an internal tool in the optimization functions since it is employed to simulate the effect of control actions on the state of the system and determines, if a new switching state of local voltage controllers (LVCs) is to be implemented [11]. Therefore, accurate and computationally efficient integration of LVCs in the power flow is essential for the efficient implementation of DMS optimization functions. The proposed SVR model can constitute an important tool in DMS applications, due to its high accuracy and its ability to maintain the structure of Y_{BUS} matrix constant saving significant computation time.

Another important application of DMS is the state estimation and monitoring of the distribution system. It is realized through the execution of power flow considering the different time delays of the LVCs of the network. More specifically, LVCs do not react instantaneously but they are assigned to react with different reaction delays [18] [19]. For instance, an SVR placed near the substation may react faster after a voltage violation occurs than an SVR placed in a farther distance. Moreover, LVCs are assigned different voltage bandwidths, inside which the LVC state remains unchanged. Depending on the reaction sequence of LVCs, the power flow could yield multiple solutions, with all of them satisfying the voltage constraints. Therefore, in order to find the most probable power flow solution in networks with LVCs, the actual reaction sequence of the LVCs should be considered based on their time delays, voltage settings and bandwidths. This process requires the execution of power flow many times by subsequently varying the taps of LVCs based on their reaction time delays, until the final state is reached [18] [19]. With the existing SVR models so far, a high amount of computation time would be required, due to the continuous refactorization of Y_{BUS} matrix every time that a tap variation occurs. This limitation is completely addressed with the proposed SVR model.

1.5 Paper structure

The rest of the paper is structured as follows: Section 2 explains the difference between the impedance value of an autotransformer and a two-winding transformer. Section 3 presents the proposed SVR model, while Section 4 explains how it is integrated in the Z-Bus power flow. Section 5 validates the proposed SVR model against Simulink and OpenDSS. Section 6 presents an analytical case study, in which the performance of the proposed SVR model is highlighted in the IEEE 8500-network. Finally, section 7 concludes the paper.

2. Impedance of autotransformers

Before we proceed with the analysis of the proposed SVR model, it is important to clarify the difference between a two separate winding transformer and an autotransformer. Fig. 1 depicts an ideal two-winding transformer and an ideal autotransformer. The impedances of the transformers are denoted as Z_{2wT} and Z_{auto} and they include the total leakage impedance of the primary and secondary winding referred to the secondary winding. The primary voltage (V_1), the secondary voltage (V_2) and the number of turns of the primary windings (N_1) are identical for both transformers.

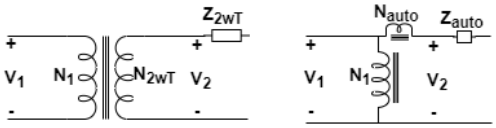

Fig. 1. Two-winding transformer (left) and autotransformer (right).

Voltages and turn numbers for the two types of transformers can be determined according to (1) and (2).

$$\frac{V_2}{V_1} = \frac{N_{2wT}}{N_1} \Longrightarrow N_{2wT} = \frac{V_2}{V_1} \cdot N_1 \qquad (1)$$

$$\frac{V_2}{V_1} = \frac{N_{auto}+N_1}{N_1} \Longrightarrow N_{auto} = \frac{V_2}{V_1} \cdot N_1 - N_1 \qquad (2)$$

It can be observed that the number of turns of secondary windings (N_{2wT} and N_{auto}) differs for the two transformer

types. Furthermore, assuming that the two transformers have an equal magnetic reluctance, the corresponding impedance ratio for the two transformer types is given by (3).

$$\frac{Z_{auto}}{Z_{2wT}} = \left(\frac{N_{auto}}{N_{2wT}}\right)^2 \quad (3)$$

By combining (1)-(3), (4) is derived, which gives the impedance ratio of the two types of transformer, as a function of the output/input voltage ratio (V_2/V_1).

$$\frac{Z_{auto}}{Z_{2wT}} = \left(\frac{\frac{V_2}{V_1}-1}{\frac{V_2}{V_1}}\right)^2 \quad (4)$$

Fig. 2 depicts the impedance ratio of the two transformer types with respect to the output/input voltage ratio. The figure is obtained using (4) for an output/input voltage ratio between 0.9 and 1.1, which is a typical voltage range for SVRs. It can be observed that the autotransformer presents significantly lower impedance than the two-winding transformer. As a result of the low impedance of the autotransformer, the Z_{BUS} power flow diverges when the compensation technique is applied to the SVR modeling [13].

3. Proposed SVR model

Fig. 3 shows an SVR of Type A in closed-delta connection. The SVR is connected between buses *p* and *s*. Z_{auto} represents the autotransformer impedance of each phase. To overcome the divergence issues resulted from the low impedance of Z_{auto}, an additional fictitious bus *m* is added in the 2-Bus circuit of Fig. 3, forming the 3-Bus circuit depicted at the top of Fig. 4. Moreover, an impedance (Z_{add}) is added in series with Z_{auto} so that $Z_{pmi} = Z_{auto} + Z_{add}$ for $i = \{a, b, c\}$. To cancel out the influence of the impedance Z_{add}, an impedance of opposite value ($-Z_{add}$) is also added in series so that $Z_{msi} = -Z_{add}$. The additional impedances Z_{add} and $-Z_{add}$ do not affect the power flow results since they are connected in series with opposite signs, thus they cancel each other. Nevertheless, they significantly enhance the power flow convergence, enabling the compensation technique to be applied in the SVR modeling.

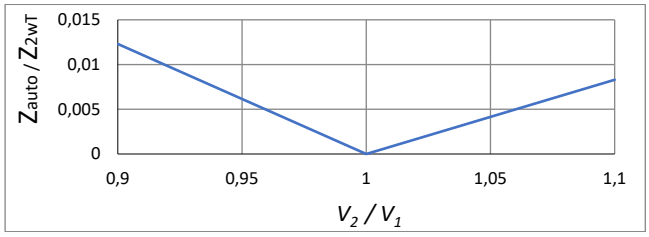

Fig. 2. Impedance ratio with respect to the output/input voltage ratio.

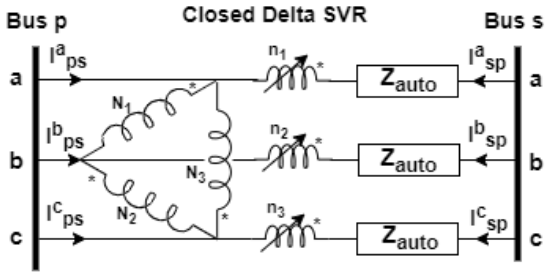

Fig. 3. Conventional 2-Bus circuit of type A SVR in closed-delta formation.

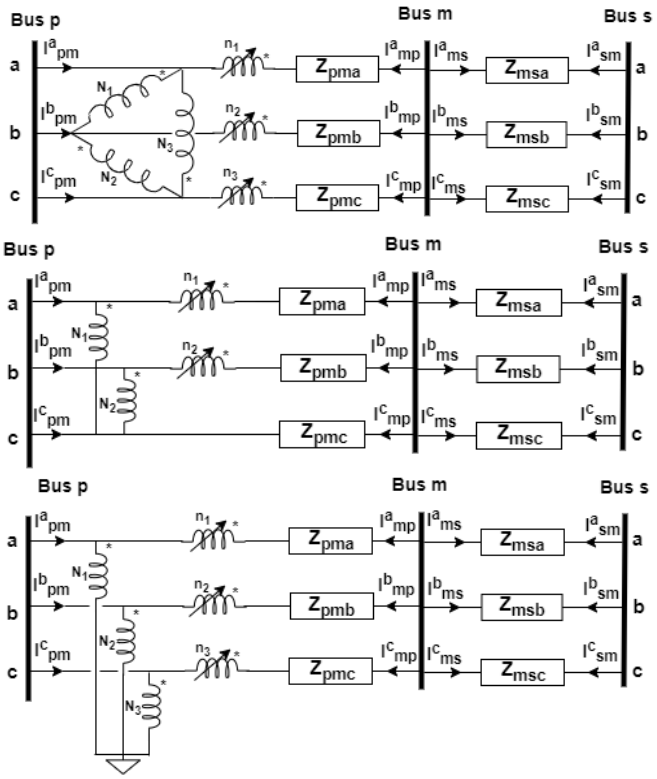

Fig. 4. Proposed 3-Bus circuits for SVRs of type A. From top to bottom: a) Closed-delta, b) Open-delta, c) Wye configuration.

By applying simple circuit analysis in Fig. 4, (5a) and (5b) are derived:

$$\begin{bmatrix} \boldsymbol{I_{pm}} \\ \boldsymbol{I_{mp}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y_{pm}} \cdot (\boldsymbol{I_d} + \boldsymbol{K}) & -\boldsymbol{Y_{pm}} \\ -\boldsymbol{Y_{pm}} \cdot (\boldsymbol{I_d} + \boldsymbol{K}) & \boldsymbol{Y_{pm}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V_p} \\ \boldsymbol{V_m} \end{bmatrix} + \begin{bmatrix} \boldsymbol{I_N} \\ \boldsymbol{0} \end{bmatrix} \quad (5a)$$

$$\boldsymbol{I_N} = \mathbf{A} \cdot \boldsymbol{Y_{pm}} \cdot \left(-\boldsymbol{V_m} + (\boldsymbol{I_d} + \mathbf{K}) \cdot \boldsymbol{V_p}\right) \quad (5b)$$

where the matrices $\boldsymbol{A}, \boldsymbol{K}, \boldsymbol{Y_{pm}}$ are defined in Tables 1 and 2 for all types and configurations of SVRs. $\boldsymbol{I_d}$ is a 3x3 identity matrix. Eq. (5a) is used to calculate the currents ($\boldsymbol{I_{pm}}, \boldsymbol{I_{mp}}$) and voltages ($\boldsymbol{V_p}, \boldsymbol{V_m}$,) between the nodes *p*-*m*, while (5b) is employed to calculate the current ($\boldsymbol{I_N}$) flowing through the primary windings (N_j). Note that (5a) and (5b) are generic and can be applied to any SVR by simply modifying the parameters $\boldsymbol{A}, \boldsymbol{K}, \boldsymbol{Y_{pm}}$ based on the type (A or B) and configuration (closed-delta, open-delta, wye), as shown in Tables 1 and 2. The winding ratios $\left(\frac{n_1}{N_1}, \frac{n_2}{N_2}, \frac{n_3}{N_3}\right)$ in Table 1 are related to the tap ratios (Tap_j) as follows [2]: $\frac{n_j}{N_j} =$

$0.00625 \cdot Tap_j$ for $j = \{1,2,3\}$, assuming that $Tap_j = \{-16, \dots, 0, \dots, +16\}$ and $-0.1 < \frac{n_j}{N_j} < 0.1$.

The square matrix in (5a) includes the matrix $\boldsymbol{K}$, which is not constant due to the tap variations. Therefore, it is moved outside the square matrix and (6a) is obtained, where the current sources $\boldsymbol{I_p}, \boldsymbol{I_m}$ are given in (6b).

$$\begin{bmatrix} \boldsymbol{I_{pm}} \\ \boldsymbol{I_{mp}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y_{pm}} & \boldsymbol{-Y_{pm}} \\ \boldsymbol{-Y_{pm}} & \boldsymbol{Y_{pm}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V_p} \\ \boldsymbol{V_m} \end{bmatrix} + \begin{bmatrix} \boldsymbol{I_p} \\ \boldsymbol{I_m} \end{bmatrix} \quad (6a)$$

$$\begin{bmatrix} \boldsymbol{I_p} \\ \boldsymbol{I_m} \end{bmatrix} = \begin{bmatrix} \mathbf{A} \cdot \boldsymbol{Y_{pm}} \cdot \left(-\boldsymbol{V_m} + (\boldsymbol{I_d} + \mathbf{K}) \cdot \boldsymbol{V_p}\right) + \boldsymbol{Y_{pm}} \cdot \boldsymbol{K} \cdot \boldsymbol{V_p} \\ \boldsymbol{-Y_{pm}} \cdot \boldsymbol{K} \cdot \boldsymbol{V_p} \end{bmatrix} \quad (6b)$$

Finally, the voltages and currents between the nodes *m*-*s* are expressed in (7), where the matrix $\boldsymbol{Y_{ms}}$ is given in Table 2.

$$\begin{bmatrix} \boldsymbol{I_{ms}} \\ \boldsymbol{I_{sm}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y_{ms}} & \boldsymbol{-Y_{ms}} \\ \boldsymbol{-Y_{ms}} & \boldsymbol{Y_{ms}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V_m} \\ \boldsymbol{V_s} \end{bmatrix} \quad (7)$$

Eqs. (6) and (7) can be comprehensively expressed in the form of an equivalent circuit as shown in Fig. 5. The parameters of the equivalent circuit for both types of SVR are given in Tables 1, 2, and 3. The square blocks of Fig. 5 consisting of $\boldsymbol{Y_{pm}}, \boldsymbol{Y_{ms}}$ are constant and are included in the $\boldsymbol{Y_{BUS}}$ matrix. The tap variables are comprised in the current sources, outside the $\boldsymbol{Y_{BUS}}$ matrix.

As shown in Table 3, the current sources depend on the matrices $\boldsymbol{Y_{pm}}, \boldsymbol{Y_{ms}}$. To ensure the convergence of the power flow, the values of these matrices should be sufficiently small so that the current sources do not take an extremely large value. That is achieved by selecting a sufficiently large value of Z_{add}. Essentially, the role of Z_{add} is to enhance the convergence by artificially increasing the value of Z_{auto}.

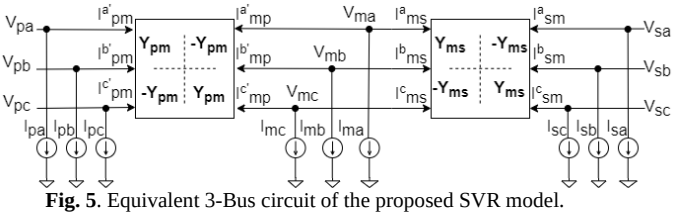

Fig. 5. Equivalent 3-Bus circuit of the proposed SVR model.

Table 1
Matrices K and A for several configurations and types of SVR

SVR Type	Matrix	Open-Delta	Closed Delta	Wye
A or B	**K**	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & -\frac{n_1}{N_1} \\ 0 & \frac{n_2}{N_2} & -\frac{n_2}{N_2} \\ 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & -\frac{n_1}{N_1} & 0 \\ 0 & \frac{n_2}{N_2} & -\frac{n_2}{N_2} \\ -\frac{n_3}{N_3} & 0 & \frac{n_3}{N_3} \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & 0 \\ 0 & \frac{n_2}{N_2} & 0 \\ 0 & 0 & \frac{n_3}{N_3} \end{bmatrix}$
A or B	**A**	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & 0 \\ 0 & \frac{n_2}{N_2} & 0 \\ -\frac{n_1}{N_1} & -\frac{n_2}{N_2} & 0 \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & -\frac{n_3}{N_3} \\ -\frac{n_1}{N_1} & \frac{n_2}{N_2} & 0 \\ 0 & -\frac{n_2}{N_2} & \frac{n_3}{N_3} \end{bmatrix}$	$\begin{bmatrix} \frac{n_1}{N_1} & 0 & 0 \\ 0 & \frac{n_2}{N_2} & 0 \\ 0 & 0 & \frac{n_3}{N_3} \end{bmatrix}$

Table 2
Y matrices for several configurations and types of SVR

Type	Matrix	Open-Delta	Closed-Delta	Wye
A	$\boldsymbol{Y_{pm}}$	$\begin{bmatrix} Z_{auto}+Z_{add} & 0 & 0 \\ 0 & Z_{auto}+Z_{add} & 0 \\ 0 & 0 & Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} Z_{auto}+Z_{add} & 0 & 0 \\ 0 & Z_{auto}+Z_{add} & 0 \\ 0 & 0 & Z_{auto}+Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} Z_{auto}+Z_{add} & 0 & 0 \\ 0 & Z_{auto}+Z_{add} & 0 \\ 0 & 0 & Z_{auto}+Z_{add} \end{bmatrix}^{-1}$
B	$\boldsymbol{Y_{ms}}$			
A	$\boldsymbol{Y_{ms}}$	$\begin{bmatrix} -Z_{add} & 0 & 0 \\ 0 & -Z_{add} & 0 \\ 0 & 0 & -Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} -Z_{add} & 0 & 0 \\ 0 & -Z_{add} & 0 \\ 0 & 0 & -Z_{add} \end{bmatrix}^{-1}$	$\begin{bmatrix} -Z_{add} & 0 & 0 \\ 0 & -Z_{add} & 0 \\ 0 & 0 & -Z_{add} \end{bmatrix}^{-1}$
B	$\boldsymbol{Y_{pm}}$			

Table 3
Current sources for the two types of SVR

SVR Type	$\boldsymbol{I_p}$	$\boldsymbol{I_m}$	$\boldsymbol{I_s}$
A	$\mathbf{A} \cdot \boldsymbol{Y_{pm}} \cdot \left(-\boldsymbol{V_m} + (\boldsymbol{I_d} + \mathbf{K}) \cdot \boldsymbol{V_p}\right) + \boldsymbol{Y_{pm}} \cdot \boldsymbol{K} \cdot \boldsymbol{V_p}$	$\boldsymbol{-Y_{pm}} \cdot \boldsymbol{K} \cdot \boldsymbol{V_p}$	$\mathbf{0}$
B	$\mathbf{0}$	$\boldsymbol{Y_{ms}} \cdot \boldsymbol{K} \cdot \boldsymbol{V_s}$	$\mathbf{A} \cdot \boldsymbol{Y_{ms}} \cdot (\boldsymbol{V_m} - (\boldsymbol{I_d} - \mathbf{K}) \cdot \boldsymbol{V_s}) - \boldsymbol{Y_{ms}} \cdot \boldsymbol{K} \cdot \boldsymbol{V_s}$

Table 4
Validation of the proposed model against Simulink for the type A SVR

	Open-Delta			Closed-Delta			Wye		
	|V4ab|	**|V4bc|**	**|V4ca|**	**|V4ab|**	**|V4bc|**	**|V4ca|**	**|V4an|**	**|V4bn|**	**|V4cn|**
Simulink	13183.73427	12936.56756	13430.15426	13804.36230	13261.03079	13474.00390	7835.31967	7385.21215	7417.952216
Proposed	13183.75038	12936.57385	13430.15983	13804.36244	13261.03156	13474.00456	7835.31980	7385.21264	7417.942290
OpenDSS	13183.75023	12936.56993	13430.16003	13804.36231	13261.03192	13474.00233	7835.31908	7385.21250	7417.941969

Table 5
Validation of the proposed model against Simulink for the type B SVR

	Open-Delta			Closed-Delta			Wye		
	|V4ab|	**|V4bc|**	**|V4ca|**	**|V4ab|**	**|V4bc|**	**|V4ca|**	**|V4an|**	**|V4bn|**	**|V4cn|**
Simulink	13272.17655	12969.62611	13567.70840	13974.97510	13290.82893	13590.54690	7915.22523	7403.58178	7436.69034
Proposed	13272.17802	12969.62880	13567.70988	13974.97740	13290.82899	13590.54697	7915.22509	7403.58377	7436.68188
OpenDSS	13272.17697	12969.62745	13567.71039	13974.97788	13290.82897	13590.55012	7915.22361	7403.58423	7436.68374

4. Implementation of the proposed SVR model in the Z-bus power flow: An example of a 4-Bus network

In this section, the implementation of the proposed model is practically explained in the 4-Bus network of Fig. 6a. A closed delta SVR of type A is connected between the nodes 2-3. Z_{auto} is the SVR impedance, while Z_{12i} and Z_{34i} for $i = \{a, b, c\}$ are the line impedances connecting the buses 1-2 and 3-4, respectively. The conventional SVR configuration is

shown in Fig. 6a, while the proposed SVR model is depicted in Fig. 6b. As shown, the proposed SVR model has an additional fictitious bus 5. Note that no load is connected to this fictitious bus. Buses 2, 5 and 3 correspond to buses *p*, *m* and *s* of Fig. 5, respectively. The impedance $Z_{25i} = Z_{auto} + Z_{add}$, while $Z_{53i} = -Z_{add}$ for $i = \{a, b, c\}$, as explained in Section 3. The networks of Figs. 6a and 6b are identical since $Z_{25i} + Z_{53i} = Z_{auto}$.

The network of Fig. 6b is described by (8), as follows:

$$\begin{bmatrix} \boldsymbol{I}_1 \\ \boldsymbol{I}_2 \\ \boldsymbol{I}_3 \\ \boldsymbol{I}_4 \\ \boldsymbol{I}_5 \end{bmatrix} = \begin{bmatrix} -\boldsymbol{Y}_{12} & \boldsymbol{Y}_{12} & 0 & 0 & 0 \\ \boldsymbol{Y}_{12} & -\boldsymbol{Y}_{12} - \boldsymbol{Y}_{25} & 0 & 0 & \boldsymbol{Y}_{25} \\ 0 & 0 & -\boldsymbol{Y}_{53} - \boldsymbol{Y}_{34} & \boldsymbol{Y}_{34} & \boldsymbol{Y}_{53} \\ 0 & 0 & \boldsymbol{Y}_{34} & -\boldsymbol{Y}_{34} & 0 \\ 0 & \boldsymbol{Y}_{25} & \boldsymbol{Y}_{53} & 0 & -\boldsymbol{Y}_{25} - \boldsymbol{Y}_{53} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V}_1 \\ \boldsymbol{V}_2 \\ \boldsymbol{V}_3 \\ \boldsymbol{V}_4 \\ \boldsymbol{V}_5 \end{bmatrix} \quad (8)$$

The square matrix of (8) includes the 3x3 admittance matrices of the lines between the buses 1-2 ($\boldsymbol{Y_{12}}$) and 3-4 ($\boldsymbol{Y_{34}}$) as well as the 3x3 matrices $\boldsymbol{Y_{25}}$ and $\boldsymbol{Y_{53}}$ calculated according to Table 2, where $\boldsymbol{Y_{25}}$ and $\boldsymbol{Y_{53}}$ correspond to $\boldsymbol{Y_{pm}}$ and $\boldsymbol{Y_{ms}}$, respectively. The voltage vectors of (8) for each bus $k = \{1,2,3,4,5\}$ are given by $\boldsymbol{V_k} = [V_{ka}, \ V_{kb}, \ V_{kc}]^T$. The current vectors of (8) are given in (9). Each vector $[I_{Lra}, \ I_{Lrb}, \ I_{Lrc}]^T$ for $r = \{1,2,3,4\}$ denotes the load currents of node *r*, while $[I_{ya}, \ I_{yb}, \ I_{yc}]^T$ for $y = \{2,5,3\}$ denote the compensating currents calculated by Table 3 and include the tap variables of SVRs. More specifically, $[I_{2a}, \ I_{2b}, \ I_{2c}]^T$ corresponds to $\boldsymbol{I_p}$, $[I_{5a}, \ I_{5b}, \ I_{5c}]^T$ corresponds to $\boldsymbol{I_m}$, while $[I_{3a}, \ I_{3b}, \ I_{3c}]^T$ corresponds to $\boldsymbol{I_s}$.

$$\begin{aligned} \boldsymbol{I_1} &= [I_{L1a}, \ I_{L1b}, \ I_{L1c}]^T, \\ \boldsymbol{I_2} &= [I_{L2a}, \ I_{L2b}, \ I_{L2c}]^T + [I_{2a}, \ I_{2b}, \ I_{2c}]^T, \\ \boldsymbol{I_3} &= [I_{L3a}, \ I_{L3b}, \ I_{L3c}]^T + [I_{3a}, \ I_{3b}, \ I_{3c}]^T, \\ \boldsymbol{I_4} &= [I_{L4a}, \ I_{L4b}, \ I_{L4c}]^T \\ \boldsymbol{I_5} &= [I_{5a}, \ I_{5b}, \ I_{5c}]^T \end{aligned} \quad (9)$$

Assuming that the bus 1 is the slack bus, the first three rows of (8) are removed and (10) is obtained, as follows:

$$\begin{bmatrix} \boldsymbol{I_2} \\ \boldsymbol{I_3} \\ \boldsymbol{I_4} \\ \boldsymbol{I_5} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y_{12}} & -\boldsymbol{Y_{12}} - \boldsymbol{Y_{25}} & 0 & 0 & \boldsymbol{Y_{25}} \\ 0 & 0 & -\boldsymbol{Y_{53}} - \boldsymbol{Y_{34}} & \boldsymbol{Y_{34}} & \boldsymbol{Y_{53}} \\ 0 & 0 & \boldsymbol{Y_{34}} & -\boldsymbol{Y_{34}} & 0 \\ 0 & \boldsymbol{Y_{25}} & \boldsymbol{Y_{53}} & \boldsymbol{0} & -\boldsymbol{Y_{25}} - \boldsymbol{Y_{53}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V_1} \\ \boldsymbol{V_2} \\ \boldsymbol{V_3} \\ \boldsymbol{V_4} \\ \boldsymbol{V_5} \end{bmatrix} \quad (10)$$

Subsequently, the product $[\boldsymbol{Y_{12}} \ \ \boldsymbol{0} \ \ \boldsymbol{0} \ \ \boldsymbol{0}]^T \cdot \boldsymbol{V_1}$ is removed from both equation sides of (10) and (11) is derived.

$$\begin{bmatrix} \boldsymbol{I_2} \\ \boldsymbol{I_3} \\ \boldsymbol{I_4} \\ \boldsymbol{I_5} \end{bmatrix} - \begin{bmatrix} \boldsymbol{Y_{12}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot \boldsymbol{V_1} = \begin{bmatrix} -\boldsymbol{Y_{12}} - \boldsymbol{Y_{25}} & 0 & 0 & \boldsymbol{Y_{25}} \\ 0 & -\boldsymbol{Y_{53}} - \boldsymbol{Y_{34}} & \boldsymbol{Y_{34}} & \boldsymbol{Y_{53}} \\ 0 & \boldsymbol{Y_{34}} & -\boldsymbol{Y_{34}} & 0 \\ \boldsymbol{Y_{25}} & \boldsymbol{Y_{53}} & \boldsymbol{0} & -\boldsymbol{Y_{25}} - \boldsymbol{Y_{53}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V_2} \\ \boldsymbol{V_3} \\ \boldsymbol{V_4} \\ \boldsymbol{V_5} \end{bmatrix} \quad (11)$$

By inverting the square matrix $\boldsymbol{Y_{BUS}}$ at the right-hand side of (11), equation (12) is obtained. It is noted that the square $\boldsymbol{Y_{BUS}}$ matrix consists of constant elements since the tap variables of SVR are simulated as compensating currents in the current sources $\boldsymbol{I_2}, \boldsymbol{I_3}, \boldsymbol{I_5}$. Therefore, $\boldsymbol{Y_{BUS}}$ is inverted only once and not after each tap change. Selecting a sufficiently large value of Z_{add}, the current sources $\boldsymbol{I_2}, \boldsymbol{I_3}, \boldsymbol{I_5}$ are adequately small to ensure the convergence of the power flow.

$$\begin{bmatrix} \boldsymbol{V_2} \\ \boldsymbol{V_3} \\ \boldsymbol{V_4} \\ \boldsymbol{V_5} \end{bmatrix}^{k+1} = \begin{bmatrix} -\boldsymbol{Y_{12}} - \boldsymbol{Y_{25}} & 0 & 0 & \boldsymbol{Y_{25}} \\ 0 & -\boldsymbol{Y_{53}} - \boldsymbol{Y_{34}} & \boldsymbol{Y_{34}} & \boldsymbol{Y_{53}} \\ 0 & \boldsymbol{Y_{34}} & -\boldsymbol{Y_{34}} & 0 \\ \boldsymbol{Y_{25}} & \boldsymbol{Y_{53}} & \boldsymbol{0} & -\boldsymbol{Y_{25}} - \boldsymbol{Y_{53}} \end{bmatrix}^{-1} \cdot \left(\begin{bmatrix} \boldsymbol{I_2} \\ \boldsymbol{I_3} \\ \boldsymbol{I_4} \\ \boldsymbol{I_5} \end{bmatrix}^{k} - \begin{bmatrix} \boldsymbol{Y_{12}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot \boldsymbol{V_1} \right) \quad (12)$$

Equation (12) is iteratively solved until a certain preset tolerance is reached. In (12), *k* denotes the iteration number.

5. Validation of the proposed SVR model

5.1 IEEE 4-Bus network with 1 SVR

The results of the proposed model are compared against OpenDSS (version 9.1.0.1) and Simulink (version 2018a), using the IEEE 4-Bus network. OpenDSS and Simulink were selected for the validation since they are two of the most widely-used and accurate commercial simulation softwares. The former is a powerful tool performing time-domain analysis, while the latter is a well-established software for the power flow analysis of grids. In Simulink, the SVR was formed by connecting two or three ideal transformer blocks depending on the SVR configuration e.g closed-delta, open-delta, wye. The transformers have pre-specified winding ratio to correspond with those of SVR. The impedance of SVR was modeled as an external impedance connected in series with the secondary winding, as shown in Fig. 6a. A similar rationale was followed when modeling SVRs in OpenDSS.

Some clarifications about the applied parameters are provided below:

- The unbalanced loads of [17] are used in this paper. In Open-Delta and Closed-Delta configuration the loads are phase-to-phase connected, while in wye configuration they are phase-to-neutral.
- The SVR is placed in the position of the transformer, between the buses 2-3 [17]. The impedance of the SVR (Z_{auto}) is calculated based on the data of the single-phase two-winding transformer given in [17], which has the following parameters: $V_{base} = 7.2kV$, $S_{base} = 2MVA$, $z = 0.01 + 0.06j \ (pu)$. Hence, in physical units $Z_{2wT} = 0.26 + 1.55j \ Ohm$. According to the analysis of section 2, $Z_{auto} \leq 0.01 \cdot Z_{2wT}$, thus $Z_{auto} \leq 0.0026 + 0.0155j \ Ohm$. It is noted, that although the SVR impedance varies with the tap settings of SVR, we assume it is constant. The inaccuracy introduced by this assumption is negligible, due to the very low value of Z_{auto}.
- The taps applied in the simulation are as follows: (Tap_1, Tap_2, Tap_3) = (16,8,8). Note that in open delta configuration Tap_3 does not exist.

The results of the proposed model, Simulink and OpenDSS are contrasted in Table 4 for the SVR of type A, and in Table 5 for the SVR of type B. Indicatively, only the phase-to-phase (or phase-to-neutral) voltages of the 4th bus are depicted here. The remaining buses present similar accuracy. As shown, the results of the proposed approach are in full agreement with those of Simulink and OpenDSS confirming the accuracy of the proposed model.

5.2 8-Bus network with 3 SVRs

The proposed SVR model is further validated in the 8-Bus network of Fig. 7, consisting of 3 SVRs and 4 unbalanced constant impedance loads. It is a 4-wire network with the following assumptions: 1) every bus is considered perfectly grounded, 2) the mutual impedance between the neutral and phase conductors is zero. The parameters of the network are quoted in Table 6, while the loads are given in Table 7. The taps of SVRs for the simulated configurations are presented in Table 8.

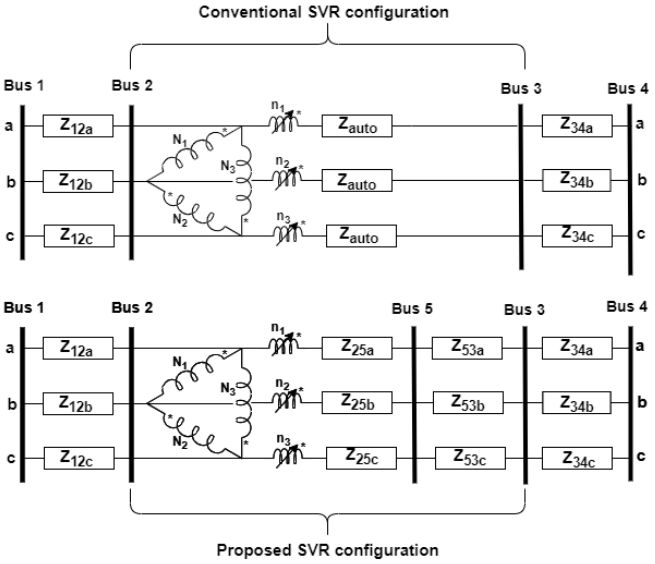

Fig. 6. From top to bottom: a) 4-Bus network with the conventional SVR configuration between the buses 2-3 and b) 4-Bus network with the proposed SVR modeling.

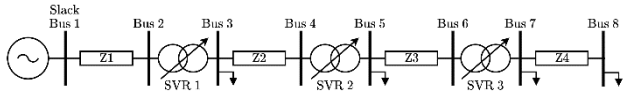

Fig 7. Unbalanced 8-Bus MV network consisting of 4 constant impedance loads and 3 SVRs.

The proposed approach is compared against Simulink and OpenDSS and the results are presented in Table 9. Indicatively, only the voltage magnitude of the three phases of bus 8 are depicted, nevertheless, the remaining buses present similar accuracy. In Table 9, the results of the proposed approach are presented in regular font, the results of Simulink in bold, while the results of OpenDSS in green color. As shown, although the network consists of 3 SVRs, the proposed model produces almost identical steady-state power flow results with Simulink and OpenDSS confirming its accuracy. Finally, the currents of the lines of the 8-bus network are shown in Table 10 for the proposed approach (regular font), Simulink (bold) and OpenDSS (green). The SVRs are in closed-delta connection of type A and their tap settings are provided in Table 8. It is confirmed that the proposed approach is very accurate since all results are identical with those of commercial softwares (γιωργο βαλε τα αποτελεσματα του OpenDSS στον table 10).

Table 6

Parameters of 8-Bus network

Distance of the lines	5 km
Phase-to-neutral Voltage of slack bus	7200 V
Frequency of the network	50 Hz
Resistance of the lines (per phase)	0.4 Ω/km
Self-reactance of the lines (per phase)	0.3 Ω/km
Mutual-reactance between phase conductors	0.1 Ω/km
Impedance of SVRs	0 Ohm

Table 7

Loads of 8-Bus network

Load Bus 3	$Z_{La} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$ $Z_{Lb} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$ $Z_{Lc} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$
Load Bus 5	$Z_{La} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$ $Z_{Lb} = 125\,\Omega \ in\ parallel\ with\ j500\,\Omega$ $Z_{Lc} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$
Load Bus 7	$Z_{La} = 150\,\Omega \ in\ parallel\ with\ j600\,\Omega$ $Z_{Lb} = 100\,\Omega \ in\ parallel\ with\ j400\,\Omega$ $Z_{Lc} = 150\,\Omega \ in\ parallel\ with\ j600\,\Omega$
Load Bus 8	$Z_{La} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$ $Z_{Lb} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$ $Z_{Lc} = 250\,\Omega \ in\ parallel\ with\ j1000\,\Omega$

Table 8

Taps of SVRs (Tap_1, Tap_2, Tap_3) for the simulated configurations

	SVR 1	**SVR 2**	**SVR 3**
Wye Type A	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)
Open Delta Type A	(8, 8, -)	(8, 8, -)	(8, 8, -)
Close Delta Type A	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)
Wye Type B	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)
Open Delta Type B	(8, 8, -)	(8, 8, -)	(8, 8, -)
Close Delta Type B	(8, 10, 8)	(8, 10, 8)	(8, 10, 8)

Table 9

Phase-to-neutral voltages for the 8-Bus network calculated with the proposed method, Simulink and OpenDSS for several SVR configurations

	Phase A	**Phase B**	**Phase C**
Wye Type A	7331.1433 **7331.1831** **7331.0209**	7244.2791 **7244.3462** **7244.2303**	7450.4267 **7450.4712** **7450.3029**
Open Delta Type A	7784.6505 **7784.6936** **7784.6967**	7576.6246 **7576.7013** **7576.5696**	6468.4454 **6468.4729** **6468.5091**
Close Delta Type A	7799.5715 **7799.5704** **7799.4528**	7845.3272 **7845.3521** **7845.2551**	7880.3313 **7880.3782** **7880.1900**
Wye Type B	7377.7522 **7377.7209** **7377.6269**	7312.6066 **7312.6144** **7312.5579**	7500.9205 **7500.9656** **7500.7956**
Open Delta Type B	7858.3033 **7858.3470** **7858.1504**	7649.9001 **7649.9796** **7649.7734**	6463.4446 **6463.4717** **6463.4885**
Close Delta Type B	7874.3123 **7874.3141** **7874.3046**	7960.3695 **7960.3946** **7960.4086**	7948.5619 **7948.6069** **7948.5285**

Table 10

Line currents for the 8-Bus network calculated with the proposed method, Simulink and OpenDSS for the closed-delta configuration

	Phase A	**Phase B**	**Phase C**
Line 1-2	175.6681 **175.6643**	248.2772 **248.2724**	186.0943 **186.0901**

	175.6800	**248.2830**	**186.1130**
Line 3-4	133.2405 **133.2377** **133.2480**	199.8065 **199.8026** **199.8100**	139.1992 **139.1960** **139.2100**
Line 5-6	92.8176 **92.8156** **92.8207**	123.2700 **123.2677** **123.2720**	95.2407 **95.2385** **95.2449**
Line 7-8	32.1585 **32.1577** **32.1580**	32.3471 **32.3464** **32.3468**	32.4914 **32.4906** **32.4909**

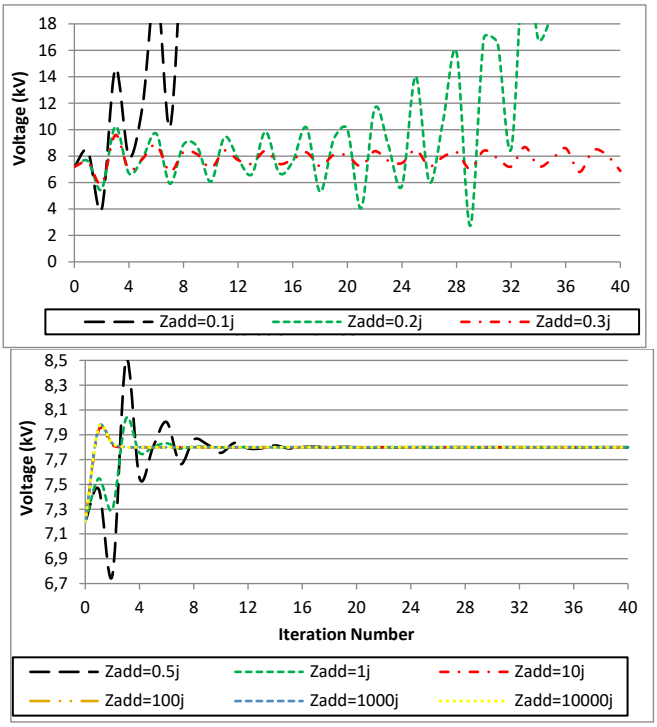

Fig. 8. Voltage of phase A of the last bus of the 8-bus network, during the iterative power flow process. SVRs are in closed-delta and type A connection. From top to bottom: a) low Zadd values, b) large Zadd values

5.3 Convergence properties of the proposed SVR model

The convergence characteristics of the proposed model are presented here, with respect to the values of the additional impedance Z_{add} introduced in Section 3. Fig 8 depicts indicatively the voltage of phase A at the last bus of the 8-bus network, throughout the iterative process of power flow, for several values of Z_{add}. More specifically, Fig. 8a depicts the voltage for low values of Z_{add} (from 0.1j to 0.3j), while Fig. 8b for high values (from 0.5j to 10000j). Although Z_{add} takes only inductive values in Fig. 8, similar results are derived with resistive values of similar magnitude. It is clarified that a flat start was considered for all the nodes of the network. Based on the figure, the following observations are derived:

- For low Z_{add} values (see Fig. 8a) the Z-Bus power flow diverges. It occurs because for low Z_{add} values, the matrices $\boldsymbol{Y_{pm}}, \boldsymbol{Y_{ms}}$ are increased (see Table 2). As a result, the current sources of Fig. 5 (see Table 3) are increased as well, resulting in the divergence of the power flow.
- The algorithm presents fast convergence for all $Z_{add} \geq 0.5j$, as shown in Fig. 8b. Thus, Z_{add} can be arbitrarily selected over a very wide range of values, making the selection of a proper Z_{add} value a very simple process.
- The algorithm converges to the same solution for all $Z_{add} \geq 0.5j$. This is logical since an impedance $-Z_{add}$ is connected in series with Z_{add} (see section 3), canceling completely the influence of Z_{add}. In fact, Z_{add} is added to reduce the values of the current sources of Table 3, and therefore, enhance the convergence of the power flow, without affecting the power flow results.

6. Performance of the proposed model in a real network with various local controllers

6.1 Description of the network

The performance of the proposed SVR model is tested in the IEEE 8500-Node network, which is a real large-scale distribution network. It includes originally 4 SVRs and 4 capacitor banks. SVR 1 is assumed to be connected in wye configuration, SVR 2 in open delta configuration, while SVRs 3 and 4 are connected in closed delta configuration. SVR 1, SVR 2, SVR 3 and SVR 4 are connected between the buses 1-2, 405-406, 1057-1058 and 1311-1312, respectively. The capacitors have been connected in buses 15, 146, 644 and 1298. The topology of IEEE 8500-network is shown in Fig. 9. In order to investigate the interactions of SVRs with the DGs, we connected 4 DGs to the buses 100, 350, 835 and 1600.

To get a sense about the position of each bus inside the network, their distance from the substation is presented in Fig. 10. More details about the data of the network e.g lines, loads are provided in [17]. All buses of the network are considered perfectly grounded.

6.2 Modeling of the local voltage controllers

Switched capacitors in distribution networks usually operate in voltage or reactive power control. In voltage control mode, the controller switches the capacitor ON when the measured voltage is less than a minimum value and OFF when it is more than a maximum value [22]. In reactive power mode, the capacitor is switched depending on the reactive power value and direction through the supervised line. In power flow formulation, capacitors are simply modeled as constant impedance loads with $Z_c = (j\omega C)^{-1}$. In this study, all capacitor banks are assumed to operate in voltage control mode, and all have the same capacitances. The capacitance of each phase is given in Table 12.

The steady state modeling of DGs is usually categorized depending on the generated voltage/current profile as well as the power profile, as follows:

1. *Voltage and current profile.* Inverter-based DGs can generate balanced phase-to-phase voltage, balanced phase-to-neutral voltage, or balanced current. On the contrary, the synchronous generator-based DGs present nonzero finite negative- and zero-sequence admittances, thus they usually generate unbalanced voltages and currents [6].

2. *Power profile.* DGs can operate in constant PQ, constant voltage (conventional PV bus modeling), or constant P-Q(V) mode [23] [24].

In this study, the DGs are assumed to generate different current and voltage profiles as shown in Table 11. The active power and the droop gains of DGs 2 and 3 are provided in Table 12.

6.3 Switching delays of local voltage controllers

LVCs are usually configured to react with pre-specified time delays. This is done in order to coordinate the switching actions of LVCs and to avoid unnecessary switchings, due to the temporary voltage variations.

The switching capacitors are set with an intentional time delay such that the capacitor switching is activated, after a pre-specified time delay, from the instant that a voltage violation is sensed [18] [19] [25]. The intentional time delay, as well as the reference voltage and bandwidth of capacitors are quoted in Table 12.

Similarly, SVRs step the voltage up or down when a voltage violation occurs beyond a pre-specified bandwidth, considering a pre-specified time delay. More specifically, as soon as a voltage violation is detected, the intentional time delay is counted before the first step-up/down switching action. If the voltage remains outside the bandwidth, additional step-up/down actions are executed with a mechanical delay [18] [19]. The intentional and mechanical time delay, as well as the reference voltage and bandwidth of SVRs are quoted in Table 12.

DGs present a very fast reaction time compared to the intentional or mechanical delays of the other LVCs. Thus, it is assumed that they react instantaneously to any load/generation variation [25]-[28].

It is clarified that the intentional time delays of capacitors and SVRs were selected based on their distance from substation. Near to substation LVCs have shorter intentional time delays [29, page 29], and it is increased for longer distances.

Switching capacitors, SVRs, and OLTCs can operate in two different ways: a) their three-phases are independently controlled; thus, each device has three local controllers acting independently on each phase, or b) each device has one local controller, which controls the three phases simultaneously [30]-[32]. In thus study, we assume that each phase is independently controlled.

6.4 Power flow algorithms for distribution networks with local controllers

For safe, reliable, and efficient operation, distribution management systems (DMS) regularly carry out optimization functions such as Volt/Var control (VVC) and optimal feeder reconfiguration (OFR), which require precise power flow solutions with accurate modeling of LVCs. Therefore, accurate modeling of LVCs in power flow studies is essential to understand their interactions in the distribution network and have appropriate understanding of the power system states.

The inclusion of the LVCs into the power flow is known to create multiple power flow solutions, as a result of the different reaction speed of LVCs and the discrete switching states of SVRs, OLTCs and capacitor banks. The state of-the-art for simulating local voltage controllers computes the most likely operational solution by considering the different precedence of the controlled devices, according to their reaction time delays [11].

The time delays of LVCs were introduced for the first time into the power flow studies in 2000 by a research group of Siemens [33] and it is considered the state-of-the-art so far in the steady state modelling of distribution networks with LVCs. More specifically, LVCs were divided into different groups based on their switching time delays. The LVCs with the fastest reaction belong to the first group, while the slowest ones belong to the last group. The method of [33] was improved later in [7] [11] by introducing sensitivity parameters to accelerate the convergence of the power flow. In the aforementioned approaches, a single-phase power flow is applied neglecting the network unbalances.

Authors in [18] [19] developed a three-phase power flow algorithm, which precisely considers the actual switching sequence of LVCs based on their switching time delays. Moreover, it considers the various operational modes of DGs as well as the unbalances that usually exist in distribution networks. In this case study, we applied the method of [18] [19] for calculating the power flow of the examined 8500-node network considering the LVCs and DG characteristics of Tables 11 and 12.

6.5 Power flow results

Initially, the power flow is executed considering all the LVCs at their initial switching state. In this example, the taps of all SVRs are initially assumed at 0 position, while the capacitors are OFF. After the convergence of the power flow (at 43^{th} iteration), the voltages of LVCs are checked and a switching action is undertaken from the LVCs with the shortest time delay that violate their voltage bandwidth. Then, the power flow is executed again, the voltages of LVCs are re-checked and a switching action is activated in order of priority, until all voltages lie inside their bandwidth and no other switching actions are required.

All switching actions of the examined network are summarized in Table 13 and explained below. The algorithm converges in 309 iterations. The proposed model as well as the three-phase model of [1] are applied for the modelling of SVRs and the results of both models are discussed in the next sub-section.

Switching action 1: The first switching action is taken over by the SVR 1 since it violates its voltage bandwidth and has the shortest time delay. More specifically, SVR 1 step up the voltage of all phases by one tap in order to increase its voltage toward its bandwidth.

Switching actions 2-6: After the first switching action of SVR 1, its voltage remains below the bandwidth. Therefore, SVR1 step up the voltage of all phases sequentially, with a mechanical time delay, until the voltages of all phases lie inside bandwidth, as shown in Fig. 15.

Switching actions 7: SVR 3 steps up its voltage by one tap after 60 sec (the time delay of SVR 3).

Switching actions 8-10: The voltage of SVR 3 still remains below its bandwidth and additional step-up functions are

performed with a mechanical time delay for the phases that violate the voltage, as depicted in Fig. 17.

Switching actions 11: The three phases of capacitor bank 4 are switched ON after the time delay of 75 seconds (it corresponds to 213th iteration), as shown in Fig. 14.

Switching actions 12: The three-phases of SVR 4 lie outside the bandwidth resulting in a switching action after the time delay of 90 seconds.

Switching actions 13-16: SVR 4 undertakes sequential switching actions with a mechanical time delay for the phases with a violated voltage, until all voltages are inside bandwidth, as shown in Fig. 18.

Switching actions 17: At 135s, phase B of capacitor 2 is switched ON. It occurs because the step-up function of SVR 4 at 90s caused a reduction at the reactive power of DG 4 (see Fig. 19), which in turn forced the voltage of phase B of capacitor 2 below its bandwidth. As a result, a switching action is taken over from Capacitor 2 after the time delay of 45s, namely at 135s.

Switching actions 18: Similarly, with the switching action 17, the switching action 18 is activated at 139 s, due to the voltage violation of phase A of capacitor 2 at 94 s, as shown in Fig. 12.

Switching actions 19: The step-up action of SVR 4 at 92s cause a reduction of the reactive power of DG 4 (see Fig. 19), which in turn cause a voltage violation of phases A and B of SVR 3. As a result, a step-up function is performed by the phases A and B after the time delay of 60s, namely at 152 s.

Switching actions 20-22: SVR 3 undertakes additional step-up functions with a mechanical delay until the voltage of all phases lie inside the bandwidth, as depicted in Fig. 17.

Switching actions 23: Due to the switching action of phase B of capacitor 2 at 135 s, the reactive power of DG 1 (see Fig. 19) is reduced forcing the voltage of phase C of capacitor 2 below its bandwidth. Thus, phase C of capacitor 2 is switched ON 45s later at 180s, as depicted in Fig. 12.

6.6 Discussion about the power flow results

The voltage profile of the network after all LVC switching actions have been executed is depicted in Fig. 20, using the proposed model as well as the model of ref. [1] for the simulation of SVRs. The two models produce exactly the same results confirming the accuracy of the proposed model.

However, a huge difference is observed in the computation time of the two models. As shown in Table 13, 19 switching actions are executed in the examined case study by the SVRs until their voltage is stabilized inside their bandwidths. The model of [1] includes the taps of SVRs in the Y_{BUS} matrix, and therefore, the re-factorization (or inversion) of the Y_{BUS} matrix is executed 19 times during the power flow process. On the opposite, the proposed model simulates the taps as fictitious current sources and the Y_{BUS} matrix remains constant throughout the whole power flow process. As a result, the power flow is executed in only 154.5s using the proposed SVR model (0.5s per iteration for 309 iterations) and in 1408.5s using the model of [1]. It is clarified that the inversion of the Y_{BUS} matrix of the examined network is performed in around 66s in Matlab, due to the large size of the network. A summary of the computation time of the power flow for the two SVR models is provided in Table 14. All simulations were conducted in a PC with an Intel Core i7, 3.4GHz CPU and 16GB DDR3 RAM.

Finally, another important thing to note in Figs 11-19 is the fast convergence of the power flow when the proposed SVR model is applied. More specifically, the power flow converges very fast to the new solution after each SVR tap variation. Although the proposed model uses fictitious current sources to simulate the taps of SVRs, the convergence of power flow is not compromised.

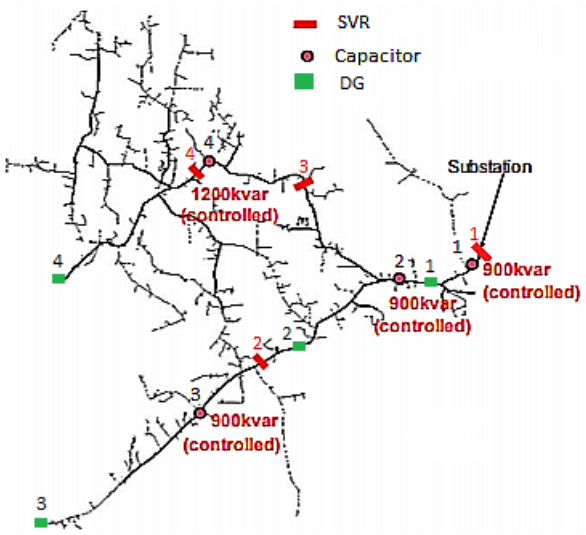

Fig 9. The IEEE 8500-node network. It consists of 4 capacitor banks and 4 SVRs. The outputs of the SVRs are connected to the following buses: SVR 1→Bus 2, SVR 2→Bus 406, SVR 3→Bus 1058, SVR 4→Bus 1312. The capacitors are connected as follows: CAP 1→Bus 15, CAP 2→Bus 146, CAP 3→Bus 644, CAP 4→Bus 1298. The DGs are connected as follows: DG 1→Bus 100, DG 2→Bus 350, DG 3→Bus 835, DG 4→Bus 1600.

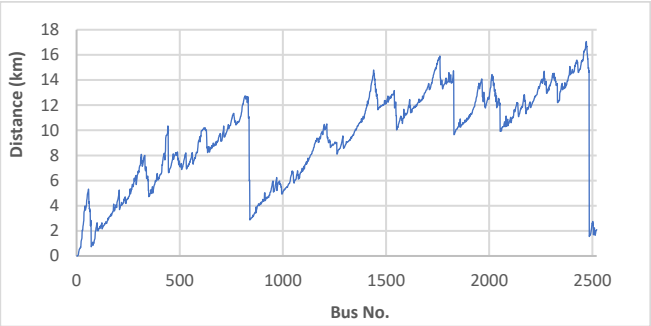

Fig 10. Distance of the buses of the IEEE 8500-node network from the substation [6, supplementary material].

Table 11
DG parameters

DG #	Power profile	Connecting Bus	Voltage/Current profile
1	Constant PV	100	SG (Unbalanced voltage and current)
2	Droop Q(V)	350	Balanced Current
3	Droop Q(V)	835	Balanced Current
4	Constant PV	1600	Balanced Voltage

Table 12
Parameters of the Modified IEEE 8500-Node Network

Data about the lines	Given in [13]
Data about the loads	Given in [13]
Voltage of slack bus	7200 V

Frequency of the network	50 Hz
Reference voltage of SVRs	7500 V
Bandwidth of SVRs	70 V
Intentional delay of SVR 1	15 s
Intentional delay of SVR 2	60 s
Intentional delay of SVR 3	60 s
Intentional delay of SVR 4	90 s
Mechanical delay of SVRs	2 s
Intentional delay of CAP 1	30 s
Intentional delay of CAP 2	45 s
Intentional delay of CAP 3	75 s
Intentional delay of CAP 4	75 s
Reference voltage of CAPs	7600 V
Bandwidth of CAPs	300 V
Capacitance of each phase	$2 \cdot 10^{-5}$ F
Active power of DGs	2 MW
Apparent power limit of DGs 1	13 MVA
Apparent power limit of DGs 2 & 3	3 MVA
Apparent power limit of DGs 4	10 MVA
Reference voltage of DGs (V_{ref})	7500 V
Droop gain of DGs 2 & 3 (K_q) [23]	10^{-4} V/Var

Table 13
Switching actions of the local voltage controllers of IEEE 8500-node network.

Number of switching action	Local Controller	Phase	Switching time	Type of switching	Iteration No.
1	SVR 1	ABC	15 s	Step Up	43
2	SVR 1	ABC	17 s	Step Up	68
3	SVR 1	ABC	19 s	Step Up	91
4	SVR 1	ABC	21 s	Step Up	111
5	SVR 1	ABC	23 s	Step Up	131
6	SVR 1	ABC	25 s	Step Up	148
7	SVR 3	ABC	60 s	Step Up	165
8	SVR 3	ABC	62 s	Step Up	180
9	SVR 3	ABC	64 s	Step Up	193
10	SVR 3	AB	66 s	Step Up	204
11	CAP 4	ABC	75 s	Switch ON	213
12	SVR 4	ABC	90 s	Step Up	222
13	SVR 4	AB	92 s	Step Up	229
14	SVR 4	AB	94 s	Step Up	236
15	SVR 4	A	96 s	Step Up	242
16	SVR 4	A	98 s	Step Up	248
17	CAP 2	B	135 s	Switch ON	254
18	CAP 2	A	139 s	Switch ON	261
19	SVR 3	AB	152 s	Step Up	269
20	SVR 3	A	154 s	Step Up	275
21	SVR 3	A	156 s	Step Up	271
22	SVR 3	A	158 s	Step Up	287
23	CAP 2	C	180 s	Switch ON	293

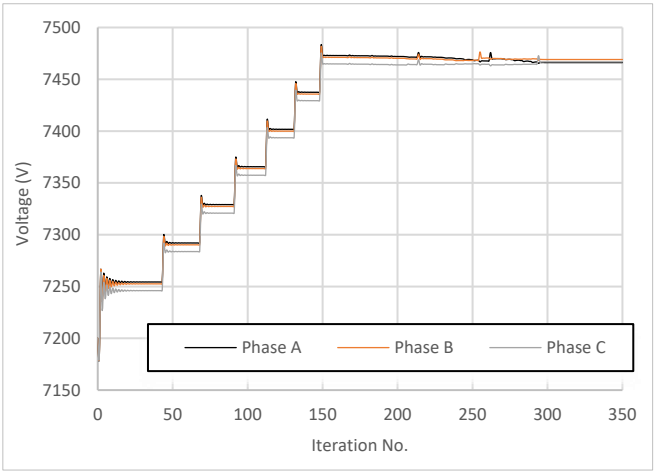

Fig 11. Voltage of capacitor 1 throughout the iterative power flow process.

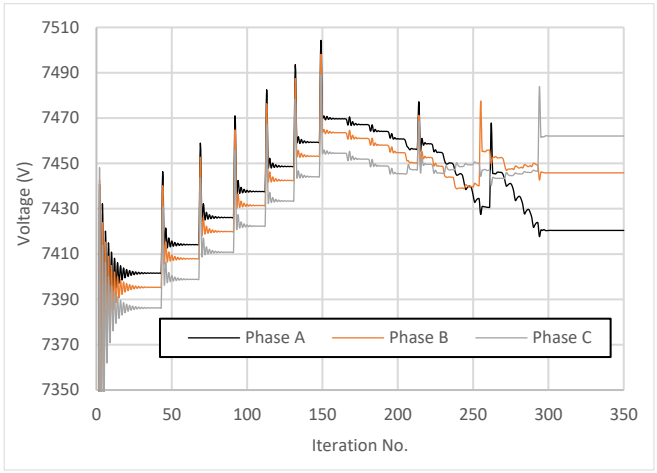

Fig 12. Voltage of capacitor 2 throughout the iterative power flow process.

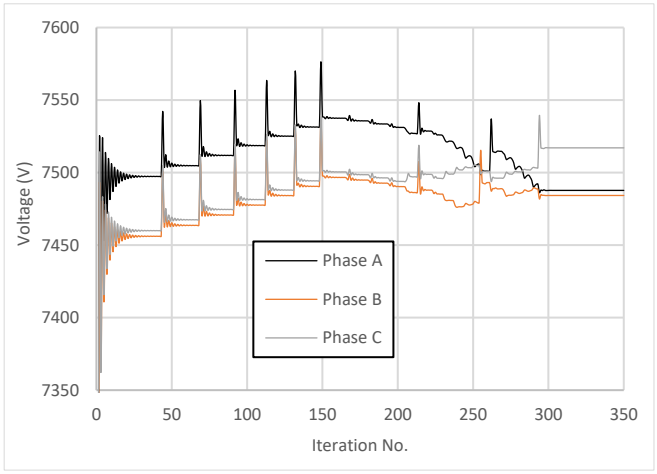

Fig 13. Voltage of capacitor 3 throughout the iterative power flow process.

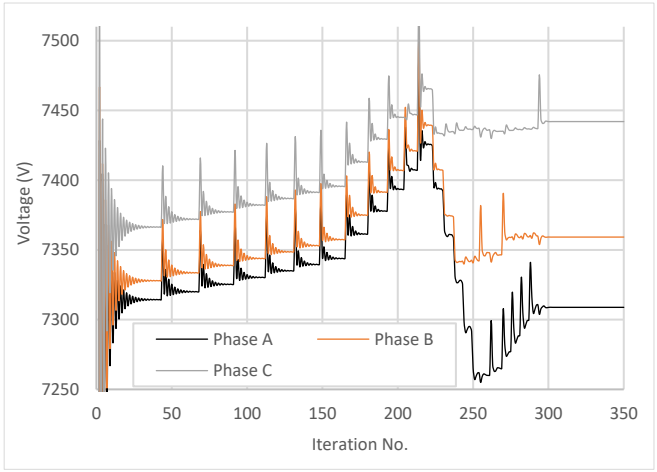

Fig 14. Voltage of capacitor 4 throughout the iterative power flow process.

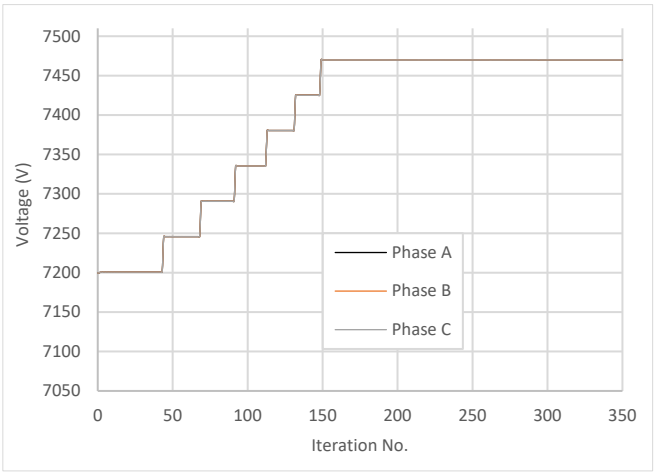

Fig 15. Voltage of SVR 1 throughout the iterative power flow process.

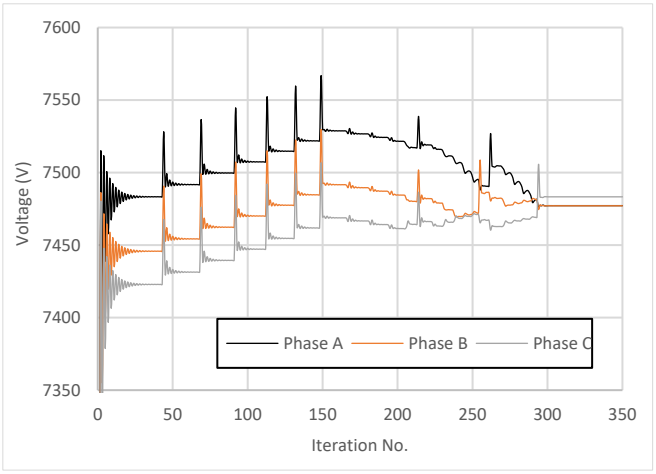

Fig 16. Voltage of SVR 2 throughout the iterative power flow process.

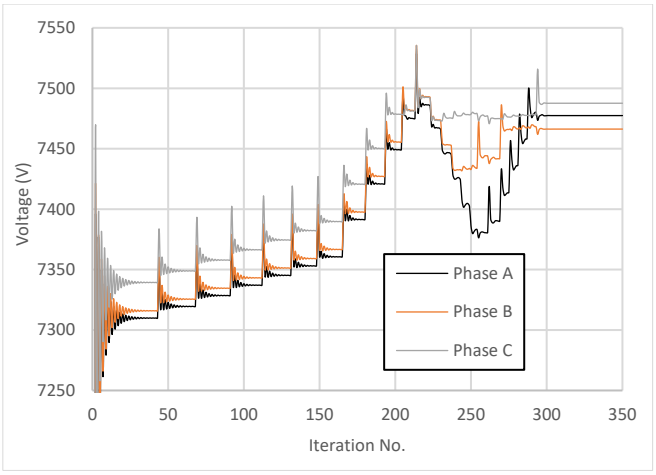

Fig 17. Voltage of SVR 3 throughout the iterative power flow process.

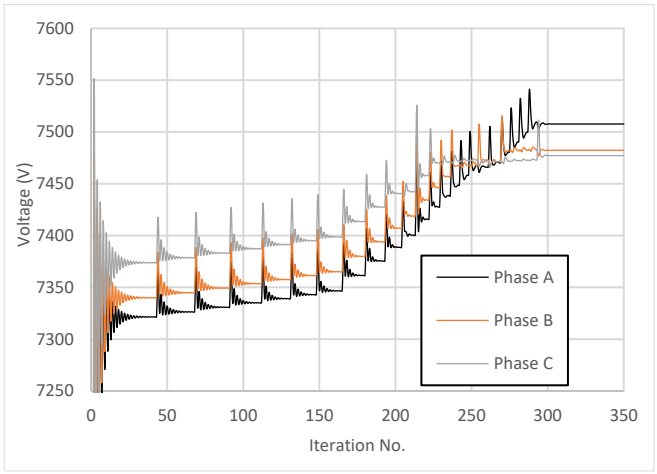

Fig 18. Voltage of SVR 4 throughout the iterative power flow process.

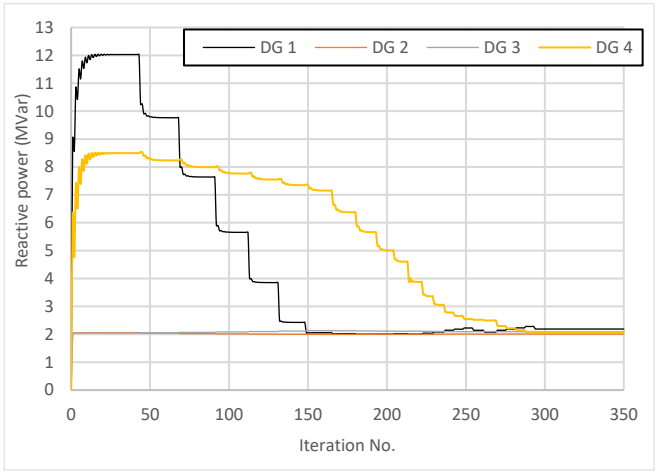

Fig 19. Reactive power of DGs throughout the iterative power flow process.

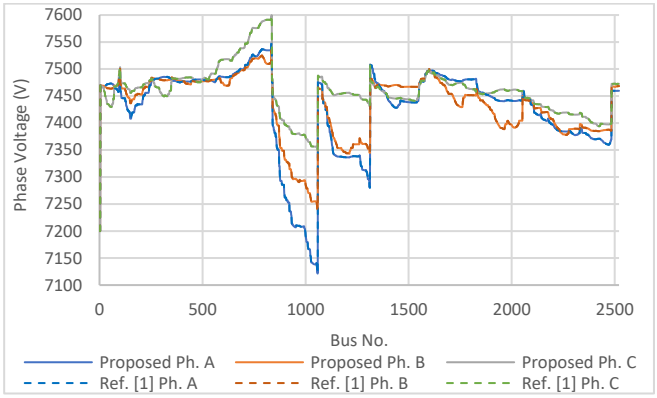

Fig 20. Voltage Profile of the network after all switching actions have been executed. The proposed model and the model of ref. [1] is applied for the simulation of SVRs.

Table 14
Total computation time of the power flow using the proposed and the model of ref. [1] for the simulation of SVRs.

	Proposed	**Ref. [1]**
Computation time of power flow iterations	154.5s (309 x 0.5s)	154.5s (309 x 0.5s)
Computation time of the inversion of the Y_{BUS} after each SVR tap variation	0s	1254s (19 x 66s)
Total computation time	154.5s	1408.5s

7. Conclusion

This paper presents a novel 3-Bus equivalent circuit for modeling three-phase SVRs in the Z_{BUS} power flow. The model is applicable in all SVR configurations. Its advantage is that the tap variables are expressed in the form of current sources outside the $\boldsymbol{Y_{BUS}}$ matrix, avoiding its re-factorization or inversion after each tap change. Furthermore, possible convergence issues caused by the low impedance of step voltage regulators are addressed by introducing fictitious impedances, without, however, affecting the accuracy of the model. The proposed model has been compared against the conventional SVR model, (expressed as a 2-bus equivalent circuit) offering significant speed up in applications, where continuous tap variations are required. The proposed SVR model can constitute an important simulation tool in several DMS applications such as state estimation, OPF, VVC, OFR, voltage stability, heuristic optimization, in which the power flow is executed in real-time with continuously varying tap settings.

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