A Generic Power Flow Algorithm for Unbalanced Islanded Hybrid AC/DC Microgrids

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***Abstract*—This paper proposes a precise power flow algorithm for islanded hybrid AC/DC microgrids (HMGs). In our analysis, we have considered a multi-grounded unbalanced bipolar DC microgrid and a multi-grounded four-wire AC microgrid connected through one or more interlinking converters (ICs). The proposed method is based on the implicit Z_{BUS} method, presenting fast convergence and robustness regardless of the *R*/*X* ratio of the lines. It can be applied in all network configurations including highly meshed distribution systems. Numerical simulations are conducted in a 12-Bus and a 47-Bus islanded unbalanced HMG to verify the validity of the proposed power flow approach considering several distributed generator (DG) operational modes. A case study in a large 1024-Bus islanded HMG further highlights the outstanding accuracy and computational performance of the proposed approach against other existing power flow methods.**

***Index Terms*—AC/DC hybrid microgrids, Bipolar DC microgrids, Interlinking converter, Multi-grounded networks.**

I. Introduction

ENVIRONMENTAL concerns have forced the energy sector worldwide towards more clean energy sources like photovoltaics, wind farms, etc. [1]. In addition, DC components like battery storage systems, LED lighting systems, and electric vehicles are expected to play a dominant role in the future energy systems [2]. The DC components are connected into the AC network through DC/AC converters deteriorating the system efficiency. The concept of hybrid AC/DC microgrids (HMGs) allows the direct connection of DC and AC components into the network increasing the system efficiency [2], [3].

An HMG consists of one or more AC subgrids connected with DC subgrids through interlinking converters (ICs) and can operate either in islanded or grid-connected mode. A DC subgrid can be either unipolar or bipolar. The unipolar is a two-wire network with only one voltage level, while the bipolar is a three-wire network (positive, neutral, negative) with two voltage levels [3], presenting an increased power transmission capability [4]. The bipolar configuration also offers the possibility of flexible selection between two different voltage levels. Finally, in the case of a faulted pole, the loads can be reconfigured in order to be supplied by the non-faulted pole resulting in higher reliability [4].

Although HMGs are still in a pre-mature stage, they are expected to play an important role in the future. Some HMG facilities have been already established, such as the one in Griffith University [5]. The practical application of HMGs necessitates a power flow algorithm that precisely simulates the steady state operation of HMGs, considering the distinct characteristics of such systems.

Power flow simulations are essential in the design stage of HMGs for studying several issues such as DGs and ICs allocation and sizing, regulation of droop parameters, Var planning, optimum power management, contingency analysis, voltage stability etc. Furthermore, the power flow can be a fundamental tool in real time operation of HMGs by contributing to the power loss and cost optimization, supervision of several variables such as voltage, frequency, thermal limits of the lines, operational limits of DGs and ICs, prediction of system state during a planned islanding etc. [6]-[10].

The power flow of islanded HMGs introduces additional challenges, compared with the conventional networks, for the following reasons [6], [7]: 1) distribution lines present high *R*/*X* ratio, 2) there is no such a large DG to undertake the role of a slack bus, as it usually occurs in large networks [8], 3) DGs usually operate in droop control mode with various voltage characteristics, and 4) the operation of the ICs should be also taken into consideration.

Several algorithms have emerged to solve the power flow in islanded HMGs. Two sequential algorithms for solving the power flow in islanded HMGs were presented in [8] and [9], using a modified backward forward sweep method (BFS) and Newton-Raphson (NR), respectively. In [6], a unified approach is adopted by applying optimization-based techniques. The authors in [10] propose a unified approach based on the NR method, while the authors in [7] apply a generalized reduced gradient method for solving the optimization problem of power flow equations. All the aforementioned studies consider balanced AC and unipolar DC (or balanced bipolar) subgrids. However, the neglect of unbalances leads to unrealistic results in LV and MV networks, as pointed out in [11].

An algorithm based on Newton Trust Region method (NTR) is presented in [12], while the authors in [13] propose a sequence-component-based power flow approach with fast computation time for solving the power flow in unbalanced HMGs. However, they consider a simplified unipolar DC network, thus ignoring the asymmetries that may occur in a bipolar DC network. Moreover, the therein implementations employ Kron reduction in the calculation of the AC line impedance. This modification indirectly assumes that the neutral conductor is perfectly grounded along the network, leading to reduced accuracy and limited capability of studying several power quality and safety issues.

This paper proposes a generic power flow algorithm for LV and MV HMGs. The main contributions of this paper are listed below:

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- *Accurate HMG modeling*: The multi-grounded neutral conductor of AC and DC subgrids is explicitly considered, resulting in increased accuracy and applicability compared to the solutions presented in the literature.
- *Computational efficiency*: Contrary to the Newton-based approaches presented in [9], [10], [12], [13] where the Jacobian matrix must be calculated and inversed at each iteration, in the proposed method, the network admittance matrix depends only on the network frequency. Thus, it can be calculated offline, reducing this way the total execution time. Additionally, a comprehensive modeling of DGs in AC and DC subgrids is proposed, by implicitly considering the zero- and negative-sequence impedance of the DGs in the admittance matrix of the network, which further reduces the total execution time.
- *Generic applicability*: The proposed algorithm can be applied in all kind of configurations such as meshed or radial, balanced or unbalanced, 3-wire or 4-wire. Moreover, it can be applied both in grid-connected and islanded HMGs.

The rest of the paper is structured as follows: Sections II and III present two individual power flow algorithms for AC and bipolar DC networks, respectively. Section IV describes the operation of ICs, while Section V integrates the individual DC and AC algorithms into a unified model to solve the power flow of HMGs. Numerical validation results for a 12-bus and a 47-Bus unbalanced islanded HMG are provided in Section VI. The computational performance of the algorithm is assessed in Section VII. Finally, a case study of a large 1024-Bus network is presented in Section VIII that highlights the advantages of the algorithm, whereas Section IX concludes the paper.

II. Power Flow in Islanded AC Subgrids

This section is divided into five parts. Initially, the theoretical background of islanded microgrids (MGs) is shortly described. Subsequently, the concept of virtual slack bus proposed in [11] for solving the power flow in islanded MGs is reminded. Thereafter, the implicit Z_{BUS} method in its original form [14] is modified to include explicitly the neutral and ground conductors. Next, the modeling of AC loads is presented. Finally, a comprehensive modeling of DGs is proposed, which enables the incorporation of negative- and zero-sequence components of DGs into the Y_{BUS} matrix of the network, enhancing the convergence speed and robustness of the algorithm.

A) Theoretical Background of Islanded AC MGs

Islanded MGs consist of small-scale DGs, thus none of them can undertake the role of slack bus. Usually, DGs in islanded AC networks operate in droop control to equally share the total network loading. The positive sequence powers produced by each DG are given by [13]:

$$P^{ac}_{G(i)} = \frac{f_{ref\,(i)} - f}{K^{ac}_{P(i)}} \tag{1}$$

$$Q^{ac}_{G(i)} = \frac{V^{ac}_{ref\,(i)} - V^{ac}_{pos(i)}}{K^{ac}_{Q(i)}} \tag{2}$$

where f, $f_{ref(i)}$, $K^{ac}_{P(i)}$, $P^{ac}_{G(i)}$, $V^{ac}_{pos(i)}$, $V^{ac}_{ref(i)}$, $K^{ac}_{Q(i)}$ and $Q^{ac}_{G(i)}$ are the network frequency, reference frequency, frequency droop gain, positive sequence active power output, positive sequence voltage magnitude, reference voltage, voltage droop gain, and positive sequence reactive power output of DG at bus i, respectively.

B) The Concept of Virtual Slack Bus for Islanded AC MGs

The configuration of an unbalanced AC network considering the neutral conductor and grounding is shown in Fig. 1. To facilitate the power flow solution in the absence of a slack bus, a bus consisting of virtual voltage sources (e.g. $V^{ac}_{(0,a)}$ in Fig. 1) is connected to an arbitrary point of the network through freely selected impedances (e.g Z^{a}_{01} in Fig. 1). The active power flowing through the virtual slack bus is calculated by (3):

$$P^{k}_{slack} = real\left(\begin{bmatrix} \frac{V^{ac}_{(0,a)}}{Z^{a\,*}_{01}} & \frac{V^{ac}_{(0,b)}}{Z^{b\,*}_{01}} & \frac{V^{ac}_{(0,c)}}{Z^{c\,*}_{01}} & \frac{V^{ac}_{(0,n)}}{Z^{n\,*}_{01}} & \frac{V^{ac}_{(0,g)}}{Z^{g\,*}_{01}} \end{bmatrix} \begin{bmatrix} (V^{ac}_{(1,a)} - V^{ac}_{(0,a)}) \\ (V^{ac}_{(1,b)} - V^{ac}_{(0,b)}) \\ (V^{ac}_{(1,c)} - V^{ac}_{(0,c)}) \\ (V^{ac}_{(1,n)} - V^{ac}_{(0,n)}) \\ (V^{ac}_{(1,g)} - V^{ac}_{(0,g)}) \end{bmatrix}^{*} \right)^{k} \tag{3}$$

The notation of (3) corresponds to Fig. 1. The symbol * denotes the conjugate complex number, while k is the iteration number. The calculated slack power in (3) is allocated in every iteration k to the DGs based on their droop equations so that the active power flowing through the virtual slack bus is nullified [11].

Moreover, in each iteration $k+1$, the voltage of the virtual slack bus is set equal to the voltage of its adjacent bus, as calculated in the previous iteration k, according to (4):

$$[V^{ac}_{(0,a)}, V^{ac}_{(0,b)}, V^{ac}_{(0,c)}, V^{ac}_{(0,n)}, V^{ac}_{(0,g)}]^{k+1} = [V^{ac}_{(1,a)}, V^{ac}_{(1,b)}, V^{ac}_{(1,c)}, V^{ac}_{(1,n)}, V^{ac}_{(1,g)}]^{k} \tag{4}$$

The notation of (4) corresponds to Fig. 1. After the algorithm has converged, any virtual source of the virtual slack bus has obtained the same voltage as its adjacent bus according to (4). Thus, no current flows through the virtual impedances ($e.g\ Z^{a}_{01}$) and the virtual slack bus does not influence the final MG operating point.

C) Modified Implicit Z_{BUS} Method to Include Neutral and Grounding Conductors

Implicit Z_{BUS} method is a fast-convergent iterative power flow algorithm with low computation time and excellent robustness characteristics [15]. However, implicit Z_{BUS} method in its original form [14] does not explicitly consider the neutral and grounding which constitute important parts of 4-wire MV and LV MGs [11]. In this sub-section, we firstly modify the implicit Z_{BUS} method to explicitly consider into calculations the neutral and grounding, and secondly we introduce into the method the concept of virtual slack bus (see Section II-B) to enable the power flow solution in islanded MGs.

As a first step, we define the equation system for a MG with m buses, as follows:

$$\begin{bmatrix} \boldsymbol{I}^{ac}_{0} \\ \boldsymbol{I}^{ac}_{1} \\ \dots \\ \boldsymbol{I}^{ac}_{m} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y}^{ac}_{00} & \boldsymbol{Y}^{ac}_{01} & \cdots & \boldsymbol{Y}^{ac}_{0m} \\ \boldsymbol{Y}^{ac}_{10} & \boldsymbol{Y}^{ac}_{11} & \cdots & \boldsymbol{Y}^{ac}_{1m} \\ \vdots & \vdots & \cdots & \vdots \\ \boldsymbol{Y}^{ac}_{m0} & \boldsymbol{Y}^{ac}_{m1} & \cdots & \boldsymbol{Y}^{ac}_{mm} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V}^{ac}_{0} \\ \boldsymbol{V}^{ac}_{1} \\ \dots \\ \boldsymbol{V}^{ac}_{m} \end{bmatrix} \tag{5}$$

where vectors $\boldsymbol{I_i^{ac}}$ and $\boldsymbol{V_i^{ac}}$ are mathematically expressed using (6) and (7), respectively.

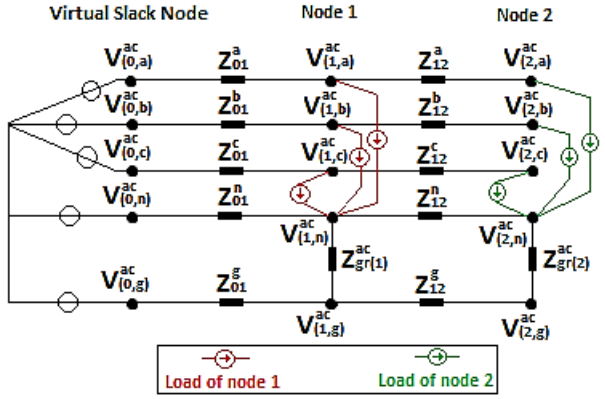

Fig. 1. Equivalent circuit of a multigrounded four-wire islanded AC MG consisting of two load buses and the virtual slack bus.

$$\boldsymbol{I_i^{ac}} = \begin{bmatrix} I^{ac}_{(i,a)} \\ I^{ac}_{(i,b)} \\ I^{ac}_{(i,c)} \\ (V^{ac}_{(i,n)} - V^{ac}_{(i,g)})/Z^{ac}_{gr(i)} - I^{ac}_{(i,a)} - I^{ac}_{(i,b)} - I^{ac}_{(i,c)} \\ -(V^{ac}_{(i,n)} - V^{ac}_{(i,g)})/Z^{ac}_{gr(i)} \end{bmatrix} \tag{6}$$

$$\boldsymbol{V_i^{ac}} = \left[V^{ac}_{(i,a)},\ V^{ac}_{(i,b)},\ V^{ac}_{(i,c)},\ V^{ac}_{(i,n)},\ V^{ac}_{(i,g)}\right]^T \tag{7}$$

The elements of (6) represent the currents that are drawn from every conductor {a, b, c, n, g} of bus *i*. $I^{ac}_{(i,r)}$ denotes the current of load or DG connected to phase r={*a*, *b*, *c*} of bus *i*. $V^{ac}_{(i,y)}$ denotes the voltage of conductor y={*a*, *b*, c, *n*, *g*} at bus *i*, according to Fig. 1.

The non-diagonal elements of the admittance matrix in (5) include the self and mutual admittances of each conductor between the buses *i* and *j*, as presented in (8).

$$\boldsymbol{Y_{ij}^{ac}} = \begin{bmatrix} Y_{ij}^{aa} & Y_{ij}^{ab} & Y_{ij}^{ac} & Y_{ij}^{an} & Y_{ij}^{ag} \\ Y_{ij}^{ba} & Y_{ij}^{bb} & Y_{ij}^{bc} & Y_{ij}^{bn} & Y_{ij}^{bg} \\ Y_{ij}^{ca} & Y_{ij}^{cb} & Y_{ij}^{cc} & Y_{ij}^{cn} & Y_{ij}^{cg} \\ Y_{ij}^{na} & Y_{ij}^{nb} & Y_{ij}^{nc} & Y_{ij}^{nn} & Y_{ij}^{ng} \\ Y_{ij}^{ga} & Y_{ij}^{gb} & Y_{ij}^{gc} & Y_{ij}^{gn} & Y_{ij}^{gg} \end{bmatrix} \tag{8}$$

The diagonal elements of the admittance matrix in (5) are defined as: $\boldsymbol{Y_{ii}^{ac}} = -\sum_{k=0,k\neq i}^{m} (\boldsymbol{Y_{ik}^{ac}})$.

Subsequently, we remove the first five rows of (5) that correspond to the virtual slack bus and (9) is obtained.

$$\begin{bmatrix} \boldsymbol{I_1^{ac}} \\ \vdots \\ \boldsymbol{I_m^{ac}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y_{10}^{ac}} & \boldsymbol{Y_{11}^{ac}} & \cdots & \boldsymbol{Y_{1m}^{ac}} \\ \vdots & \vdots & \vdots & \vdots \\ \boldsymbol{Y_{m0}^{ac}} & \boldsymbol{Y_{m1}^{ac}} & \cdots & \boldsymbol{Y_{mm}^{ac}} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V_0^{ac}} \\ \boldsymbol{V_1^{ac}} \\ \vdots \\ \boldsymbol{V_m^{ac}} \end{bmatrix} \tag{9}$$

Then, by transferring all the voltage variables of left-hand side of (9) to the right-hand side, (10) is derived.

$$\boldsymbol{I_{new}^{ac}} = \boldsymbol{Y_{new}^{ac}} \cdot \boldsymbol{V^{ac}} \tag{10}$$

Here, $\boldsymbol{V^{ac}} = [\boldsymbol{V_0^{ac}}, \boldsymbol{V_1^{ac}}, \ \ldots, \boldsymbol{V_m^{ac}}]$ while $\boldsymbol{Y_{new}^{ac}}$ is the modified admittance matrix. The $\boldsymbol{I_{new}^{ac}}$ has the form shown in (11).

$$\boldsymbol{I_{new}^{ac}} = \begin{bmatrix} I^{ac}_{(1,a)} \\ I^{ac}_{(1,b)} \\ I^{ac}_{(1,c)} \\ -I^{ac}_{(1,a)} - I^{ac}_{(1,b)} - I^{ac}_{(1,c)} \\ 0 \\ \cdots \\ I^{ac}_{(m,a)} \\ I^{ac}_{(m,b)} \\ I^{ac}_{(m,c)} \\ -I^{ac}_{(m,a)} - I^{ac}_{(m,b)} - I^{ac}_{(m,c)} \\ 0 \end{bmatrix} \tag{11}$$

Thereafter, we define the final matrices $\boldsymbol{Y_{fin1}^{ac}}$ and $\boldsymbol{Y_{fin2}^{ac}}$. The former consists of the first five columns of $\boldsymbol{Y_{new}^{ac}}$, while the latter of the remaining columns so that $\boldsymbol{Y_{new}^{ac}} = [\boldsymbol{Y_{fin1}^{ac}}\ \boldsymbol{Y_{fin2}^{ac}}]$. Eq. (12) is derived from (10) by removing $\boldsymbol{Y_{fin1}^{ac}} \cdot \boldsymbol{V_0^{ac}}$ from both sides.

$$\boldsymbol{-Y_{fin1}^{ac}} \cdot \boldsymbol{V_0^{ac}} + \boldsymbol{I_{new}^{ac}} = \boldsymbol{-Y_{fin1}^{ac}} \cdot \boldsymbol{V_0^{ac}} + \boldsymbol{Y_{new}^{ac}} \cdot \boldsymbol{V^{ac}} \tag{12}$$

Finally, (13) is directly derived from (12), where $\boldsymbol{V_{fin}^{ac}} = [\boldsymbol{V_1^{ac}}, \ldots, \boldsymbol{V_m^{ac}}]$.

$$(\boldsymbol{Y_{fin2}^{ac}})^{-1} \cdot (\boldsymbol{-Y_{fin1}^{ac}} \cdot \boldsymbol{V_0^{ac}} + \boldsymbol{I_{new}^{ac}})^k = (\boldsymbol{V_{fin}^{ac}})^{k+1} \tag{13}$$

The right-hand side of (13) is iteratively updated until all voltages have converged. Please note that $\boldsymbol{V_{fin}^{ac}}$ includes the voltage of all buses (except the virtual $\boldsymbol{V_0^{ac}}$) and all conductors including neutral and grounding.

Considering the virtual slack bus, $\boldsymbol{V_0^{ac}}$ is set in each iteration equal to the voltage of the bus that it is connected with, as explained in (4). Furthermore, the active power flowing through the virtual slack bus is assigned in every iteration to the droop-controlled DGs by updating the frequency according to (14).

$$f^{k+1} = f^k + \Delta f^k \tag{14a}$$

$$\Delta f^k = \frac{P^k_{slack}}{\sum_{i=1}^{Ndg} \frac{1}{K^{ac}_{P(i)}}} \tag{14b}$$

where P^k_{slack} is calculated from (3), while *Ndg* is the total number of droop-controlled DGs. Note that the active power of DGs is determined from the frequency according to (1). Thus, assuming that in *k* iteration $P^k_{slack} < 0$ (virtual slack bus generates active power), the frequency is reduced from (14) resulting in a rise of DGs active power from (1). In this way, the slack active power is forced to zero.

The elements of $\boldsymbol{I_{new}^{ac}}$ express either load or generation currents depending on whether a load or DG is connected in the respective bus. The mathematical modeling of loads and DGs is quoted in the last two sub-sections.

D) Modeling of AC Loads

Assuming that a load is connected to phase *a* of bus *i*, the load current is mathematically expressed, depending on the type of load and the type of connection. More specifically, wye-connected loads are connected between phase and neutral and expressed as follows:

-Wye-Constant Power: $I_{(i,a)}^{ac\ k}=S_{La}^{*}/(V_{(i,a)}^{ac\ k-1}-V_{(i,n)}^{ac\ k-1})^{*}$

-Wye-Constant Current: $I_{(i,a)}^{ac\ k}=I_0$

-Wye-Con. Admittance: $I_{(i,a)}^{ac\ k}=Y_L\cdot(V_{(i,a)}^{ac\ k-1}-V_{(i,n)}^{ac\ k-1})$

As shown, the load currents are calculated based on the voltage values of the respective bus as calculated in the previous iteration. The load current of phases *b*, *c* are calculated in a similar manner. Delta-connected loads can be modeled in a similar way. Mathematical formulations of wye- and delta-connected loads of all phases are provided in [16, Table I].

E) Modeling of AC DGs

AC DGs in microgrids can operate either in constant PQ or droop-controlled mode [13]. Synchronous generator based DGs (SG-DGs) and electronically coupled DGs (EC-DGs) present different voltage characteristics under unbalanced loading. Both SG-DGs and EC-DGs are represented by the same positive-sequence model depending on whether they operate in constant PQ or droop-mode [13].

The negative- and zero-sequence currents of EC-DGs differ from those of SGs since SG-units inherently present nonzero finite negative- and zero-sequence admittances [13]. On the other hand, EC-DGs can operate in two modes: either generating balanced voltage, thus presenting infinite negative- and zero-sequence admittances or generating balanced current, thus presenting zero negative- and zero-sequence admittances. In the following, a comprehensive model for both SG and EC-DG units is presented, as a function of their positive-sequence current components and their zero- and negative-sequence admittances.

Considering that a DG is connected to bus *i*, the positive sequence current of both SG-DGs and EC-DGs is calculated from (15a):

$$I_{pos(i)}^{ac}=\frac{P_{G(i)}^{ac}+j\cdot Q_{G(i)}^{ac}}{3\cdot V_{pos(i)}^{ac}} \tag{15a}$$

$$V_{pos(i)}^{ac}=\frac{1}{3}\cdot\left((V_{(i,a)}^{ac}-V_{(i,n)}^{ac})+a\cdot(V_{(i,b)}^{ac}-V_{(i,n)}^{ac})+a^2\cdot(V_{(i,c)}^{ac}-V_{(i,n)}^{ac})\right) \tag{15b}$$

where $P_{G(i),}^{ac}Q_{G(i)}^{ac}$ are either constant in constant PQ mode or calculated by (1), (2) in droop control mode. $V_{pos(i)}^{ac}$ is the positive-sequence component of phase-to-neutral voltage of bus *i* and calculated by (15b). Parameter α is a phasor rotation operator such that $a=e^{j\frac{2}{3}\pi}$.

The negative-sequence current is calculated as shown in (16a), as a function of the negative-sequence voltage component (described in (16b)) and the negative-sequence admittance Y_2 of DG:

$$I_{neg(i)}^{ac}=V_{neg(i)}^{ac}\cdot Y_2 \tag{16a}$$

$$V_{neg(i)}^{ac}=\frac{1}{3}\cdot\left((V_{(i,a)}^{ac}-V_{(i,n)}^{ac})+a^2\cdot(V_{(i,b)}^{ac}-V_{(i,n)}^{ac})+a\cdot(V_{(i,c)}^{ac}-V_{(i,n)}^{ac})\right) \tag{16b}$$

Similarly, the zero-sequence current is calculated as shown in (17a), as a function of the zero-sequence voltage component (described in (17b)) and the zero-sequence admittance Y_0 of DG:

$$I_{zero(i)}^{ac}=V_{zero(i)}^{ac}\cdot Y_0 \tag{17a}$$

$$V_{zero(i)}^{ac}=\frac{1}{3}\cdot\left((V_{(i,a)}^{ac}-V_{(i,n)}^{ac})+(V_{(i,b)}^{ac}-V_{(i,n)}^{ac})+(V_{(i,c)}^{ac}-V_{(i,n)}^{ac})\right) \tag{17b}$$

The currents $I_{(i,a),}^{ac}I_{(i,b),}^{ac}I_{(i,c)}^{ac}$ in (11) are written as a function of sequence components as follows:

$$I_{(i,a)}^{ac}=I_{pos(i)}^{ac}+I_{neg(i)}^{ac}+I_{zero(i)}^{ac} \tag{18a}$$

$$I_{(i,b)}^{ac}=a^2\cdot I_{pos(i)}^{ac}+a\cdot I_{neg(i)}^{ac}+I_{zero(i)}^{ac} \tag{18b}$$

$$I_{(i,c)}^{ac}=a\cdot I_{pos(i)}^{ac}+a^2\cdot I_{neg(i)}^{ac}+I_{zero(i)}^{ac} \tag{18c}$$

Equation (19a) expresses the currents of DG *i* in the form of (11). They are expressed as a function of the positive-sequence currents, the negative- and zero-sequence admittances (included in $\boldsymbol{Y_{DG}^{ac}}$ shown in (19b)) and the voltages of bus *i*. Thus, $\boldsymbol{Y_{DG}^{ac}}$ can be moved to the right side of (10) resulting in an implicit representation of negative- and zero-sequence components into the $\boldsymbol{Y_{new}^{ac}}$ matrix. The positive-sequence current component remains in the left side of (10).

$$\begin{bmatrix} I_{(i,a)}^{ac} \\ I_{(i,b)}^{ac} \\ I_{(i,c)}^{ac} \\ -I_{(i,a)}^{ac}-I_{(i,b)}^{ac}-I_{(i,c)}^{ac} \\ 0 \end{bmatrix}=\begin{bmatrix} I_{pos(i)}^{ac} \\ a^2\cdot I_{pos(i)}^{ac} \\ a\cdot I_{pos(i)}^{ac} \\ 0 \\ 0 \end{bmatrix}+\boldsymbol{Y_{DG}^{ac}}\cdot\begin{bmatrix} V_{(i,a)}^{ac} \\ V_{(i,b)}^{ac} \\ V_{(i,c)}^{ac} \\ V_{(i,n)}^{ac} \\ V_{(i,g)}^{ac} \end{bmatrix} \tag{19a}$$

$$\boldsymbol{Y_{DG}^{ac}}=\frac{1}{3}\cdot\begin{bmatrix} Y_2+Y_0 & a^2\cdot Y_2+Y_0 & a\cdot Y_2+Y_0 & -3\cdot Y_0 & 0 \\ a\cdot Y_2+Y_0 & Y_2+Y_0 & a^2\cdot Y_2+Y_0 & -3\cdot Y_0 & 0 \\ a^2\cdot Y_2+Y_0 & a\cdot Y_2+Y_0 & Y_2+Y_0 & -3\cdot Y_0 & 0 \\ -3\cdot Y_0 & -3\cdot Y_0 & -3\cdot Y_0 & 9\cdot Y_0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{19b}$$

With this process, the symmetrical components of the currents of DGs are separately treated. The positive-sequence current component is calculated in each iteration from (15a) for both SG and EC-DGs, based on the powers of droop equations and the positive-sequence voltage of the last iteration. The negative- and zero-sequence admittances (Y_0, Y_2) in (19b) are determined based on the type and control mode of DG as follows.

i. From the equations of internal negative- and zero-sequence admittances [13, eq. (6)-(7)] in SG units.
ii. $Y_0=Y_2=0$ in three- and four-wire EC-DGs with balanced generated current.
iii. $Y_0=Y_2\to\infty$ in four-wire EC-DGs with balanced generated phase-to-neutral voltage.
iv. $Y_0=0$ and $Y_2\to\infty$ in three-wire EC-DGs with balanced generated phase-to-phase voltage.

III. Proposed Method for DC Subgrids

In this section, the proposed approach for solving the power flow in DC subgrids is presented. Firstly, the theoretical background of DC MGs is provided. Secondly, the concept of virtual slack bus and the proposed power flow approach in islanded bipolar DC MGs is analyzed. Finally, the modeling of loads and a comprehensive model for DC DGs in bipolar DC MGs is developed.

A) Theoretical Background of Islanded DC MGs

Bipolar DC MGs consist of a positive, a negative and a neutral line [3]. Loads can be either pole-to-neutral or pole-to-pole connected. DGs can be connected pole-to-neutral, pole-to-pole or two-poles-to-neutral (like DG in Fig. 2). The

DGs, which are connected between two-poles-to-neutral, are usually assigned with voltage balancing functions [3], [4].

Non-dispatchable DGs are treated as constant P buses. Dispatchable DGs in islanded DC MGs operate either in *I-V* or *P-V* droop control mode and share the generated active power in the same sense as in AC MGs [9]:

$$I^{dc}_{diff\,(i)} = \frac{V^{dc}_{ref\,(i)} - V^{dc}_{diff\,(i)}}{K^{dc}_{I(i)}} \tag{20}$$

$$P^{dc}_{diff\,(i)} = \frac{V^{dc}_{ref\,(i)} - V^{dc}_{diff\,(i)}}{K^{dc}_{P(i)}} \tag{21}$$

where $I^{dc}_{diff(i)}, P^{dc}_{diff(i)}, V^{dc}_{diff(i)}$ are the DG differential mode current, power and voltage of DG at bus *i*, respectively. The differential mode component is defined in [17] and analyzed in Section III-E of this paper. As stated in [17], the differential mode component of bipolar DC networks corresponds to the positive sequence component of AC networks. $V^{dc}_{ref(i)}$ is the DG reference voltage while $K^{dc}_{I(i)}$ and $K^{dc}_{P(i)}$ are the droop gains of DG.

B) The Concept of Virtual Slack Bus for Islanded DC MGs

In the absence of a real slack bus in islanded DC MGs, a virtual slack bus is connected in the MG in the same sense as in Section II-B. The virtual slack bus consists of virtual voltage sources (e.g $V^{dc}_{(0,u)}$ in Fig. 2) connected to an arbitrarily selected bus through resistances of random values (e.g Z^{u}_{01} in Fig. 2). The voltage of virtual slack bus at iteration *k*+1 is equalized with the adjacent voltage of the iteration *k* according to (22). Please note that the notation of (22) corresponds to Fig. 2. After the algorithm has converged, the virtual slack bus has acquired the same voltage as its adjacent bus and therefore it is as if it does not exist.

$$[V^{dc}_{(0,u)}, V^{dc}_{(0,w)}, V^{dc}_{(0,n)}, V^{dc}_{(0,g)}]^{k+1} = [V^{dc}_{(1,u)}, V^{dc}_{(1,w)}, V^{dc}_{(1,n)}, V^{dc}_{(1,g)}]^{k} \tag{22}$$

C) Power Flow Analysis of Bipolar DC Islanded MGs

The full configuration of an islanded bipolar DC network is shown in Fig. 2. It consists of the virtual slack bus (bus 0), two pole-to-neutral loads (bus 1) and a two-poles-to-neutral DG (bus 2). For the sake of generality, the neutral line is considered to be grounded in every bus (except bus 0). In reality, if a bus is not grounded, an infinite grounding resistance is selected for this bus. For each bus *i*, the current vector is defined in (23), while the voltage vector in (24).

$$\boldsymbol{I^{dc}_{i}} = \begin{bmatrix} I^{dc}_{(i,u)} \\ I^{dc}_{(i,w)} \\ (V^{dc}_{(i,n)} - V^{dc}_{(i,g)})/Z^{dc}_{gr(i)} - I^{dc}_{(i,u)} - I^{dc}_{(i,w)} \\ -(V^{dc}_{(i,n)} - V^{dc}_{(i,g)})/Z^{dc}_{gr(i)} \end{bmatrix} \tag{23}$$

$$\boldsymbol{V^{dc}_{i}} = \begin{bmatrix} V^{dc}_{(i,u)} & V^{dc}_{(i,w)} & V^{dc}_{(i,n)} & V^{dc}_{(i,g)} \end{bmatrix}^{T} \tag{24}$$

The current vector of (23) includes the currents that are drawn from each conductor (*u, w, n, g*) of bus *i*. $I^{dc}_{(i,x)}$ denotes the current of DG or load connected to pole *x*={*u, w*} of bus *i*. The voltage vector of (24) contains the voltage of each conductor of bus *i*. $V^{dc}_{(i,y)}$ denotes the voltage of conductor *y*={*u, w, n, g*} at bus *i*. $Z^{dc}_{gr(i)}$ is the grounding resistance of neutral conductor at bus *i*.

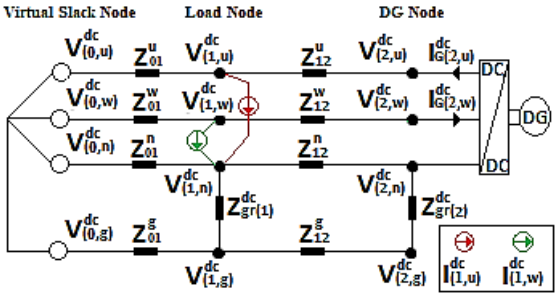

Fig. 2. Equivalent circuit of a multigrounded bipolar DC MG consisting of the virtual slack bus, a load bus, and a DG bus.

Assuming a network with *m* buses, the current vectors can be expressed as a function of the voltage vectors as follows:

$$\begin{bmatrix} \boldsymbol{I}^{dc}_{0} \\ \boldsymbol{I}^{dc}_{1} \\ \dots \\ \boldsymbol{I}^{dc}_{m} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y}^{dc}_{00} & \boldsymbol{Y}^{dc}_{01} & \cdots & \boldsymbol{Y}^{dc}_{0m} \\ \boldsymbol{Y}^{dc}_{10} & \boldsymbol{Y}^{dc}_{11} & \cdots & \boldsymbol{Y}^{dc}_{1m} \\ \vdots & \vdots & \cdots & \vdots \\ \boldsymbol{Y}^{dc}_{m0} & \boldsymbol{Y}^{dc}_{m1} & \cdots & \boldsymbol{Y}^{dc}_{mm} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V}^{dc}_{0} \\ \boldsymbol{V}^{dc}_{1} \\ \dots \\ \boldsymbol{V}^{dc}_{m} \end{bmatrix} \tag{25}$$

As a first step, the first four rows of (25) corresponding to the virtual slack bus are eliminated and (26) is obtained.

$$\begin{bmatrix} \boldsymbol{I}^{dc}_{1} \\ \vdots \\ \boldsymbol{I}^{dc}_{m} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y}^{dc}_{10} & \boldsymbol{Y}^{dc}_{11} & \cdots & \boldsymbol{Y}^{dc}_{1m} \\ \vdots & \vdots & \vdots & \vdots \\ \boldsymbol{Y}^{dc}_{m0} & \boldsymbol{Y}^{dc}_{m1} & \cdots & \boldsymbol{Y}^{dc}_{mm} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V}^{dc}_{0} \\ \boldsymbol{V}^{dc}_{1} \\ \vdots \\ \boldsymbol{V}^{dc}_{m} \end{bmatrix} \tag{26}$$

Next, we transfer the voltage variables of the current vectors (as presented in (23)) to the right side of (26), and (27) is obtained:

$$\boldsymbol{I}^{dc}_{new} = \boldsymbol{Y}^{dc}_{new} \cdot \boldsymbol{V}^{dc} \tag{27}$$

where $\boldsymbol{V^{dc}}$ is the vector $[\boldsymbol{V^{dc}_0}, \boldsymbol{V^{dc}_1}, \dots, \boldsymbol{V^{dc}_m}]$ consisting of the network voltages, while $\boldsymbol{Y^{dc}_{new}}$ is the modified admittance matrix. Subsequently, $\boldsymbol{Y^{dc}_{new}}$ is divided into two sub-matrices, namely $\boldsymbol{Y^{dc}_{fin1}}$ and $\boldsymbol{Y^{dc}_{fin2}}$. The former consists of the first four columns of $\boldsymbol{Y^{dc}_{new}}$, while the latter consists of the remaining columns of $\boldsymbol{Y^{dc}_{new}}$ so that $\boldsymbol{Y^{dc}_{new}} = [\boldsymbol{Y^{dc}_{fin1}}\ \boldsymbol{Y^{dc}_{fin2}}]$. By subtracting the term $\boldsymbol{Y^{dc}_{fin1}} \cdot \boldsymbol{V^{dc}_0}$ from both sides of (27) and multiplying both sides with $(\boldsymbol{Y^{dc}_{fin2}})^{-1}$, (28) is derived.

$$(\boldsymbol{Y^{dc}_{fin2}})^{-1} \cdot (-\boldsymbol{Y^{dc}_{fin1}} \cdot \boldsymbol{V^{dc}_0} + \boldsymbol{I^{dc}_{new}})^{k} = (\boldsymbol{V^{dc}_{fin}})^{k+1} \tag{28}$$

Here, $\boldsymbol{V^{dc}_{fin}}$ is the matrix containing all network voltages except the virtual slack bus. Eq. (28) is iteratively solved calculating the network voltages at iteration (*k*+1), based on the virtual slack bus voltage ($\boldsymbol{V^{dc}_0}$) after the update from (22). The matrices $\boldsymbol{Y^{dc}_{fin1}}$ and $\boldsymbol{Y^{dc}_{fin2}}$ consist of constant elements and hence no recalculation is required in each iteration. $\boldsymbol{I^{dc}_{new}}$ contains only the currents of (23). The calculation of the load and DG currents of $\boldsymbol{I^{dc}_{new}}$ is explained below.

D) Modeling of DC Loads

The currents of pole-to-neutral loads e.g., pole u of bus i, for iteration k, are calculated as follows:

-Constant Power: $I_{(i,u)}^{dc\ k}=P_{Lu}/(V_{(i,u)}^{dc\ k-1}-V_{(i,n)}^{dc\ k-1})$

-Constant Current: $I_{(i,u)}^{dc\ k}=I_0$

-Con. Admittance: $I_{(i,u)}^{dc\ k}=Y_{Lu}\cdot(V_{(i,u)}^{dc\ k-1}-V_{(i,n)}^{dc\ k-1})$

The currents of pole-to-pole loads (e.g pole u of bus i) for iteration k, are calculated as follows:

-Constant Power: $I_{(i,u)}^{dc\ k}=P_L/(V_{(i,u)}^{dc\ k-1}-V_{(i,w)}^{dc\ k-1})$

-Constant Current: $I_{(i,u)}^{dc\ k}=I_0$

-Con. Admittance: $I_{(i,u)}^{dc\ k}=Y_L\cdot(V_{(i,u)}^{dc\ k-1}-V_{(i,w)}^{dc\ k-1})$

E) Modeling of DC DGs

DGs of bipolar MGs can operate in either constant P mode (in grid-connected MGs) or in droop control (in islanded MGs). DC DGs can be pole-to-neutral connected (for smaller DGs), pole-to-pole connected or two-poles-to-neutral connected (like the DG in Fig. 2). Two-poles-to-neutral connected DGs are usually assigned to generate balanced pole-to-neutral voltage between the two poles to reduce the voltage asymmetries of the network [3], [4], [17].

In order to simulate the voltage balancing capability of DC DGs, symmetrical component theory similar to AC DGs is adopted. According to [17], the symmetrical components of a bipolar DC system are calculated by (30), while the inverse transformation from (31).

$$\begin{bmatrix} x_{com} \\ x_{diff} \end{bmatrix}=\frac{1}{2}\cdot\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}\cdot\begin{bmatrix} x_u \\ x_w \end{bmatrix} \tag{30}$$

$$\begin{bmatrix} x_u \\ x_w \end{bmatrix}=\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}\cdot\begin{bmatrix} x_{com} \\ x_{diff} \end{bmatrix} \tag{31}$$

In fact x_{com} and x_{diff} correspond to the common-mode and differential-mode components. It could be said that the differential-mode component of a DC system corresponds to the positive-sequence component of an AC system, while the common-mode component corresponds to the zero-sequence component.

The differential-mode current of a DC DG is calculated from (32a) using the differential voltage component of (32b). In (32a), $P_{G(i)}^{dc}$ is either pre-specified in the constant P mode or calculated by (21) in the P-V droop-controlled mode. In I-V droop control mode, the differential-mode current is directly calculated from (20).

$$I_{diff\,(i)}^{dc}=\frac{P_{G(i)}^{dc}}{2\cdot V_{diff\,(i)}^{dc}} \tag{32a}$$

$$V_{diff\,(i)}^{dc}=\frac{1}{2}\cdot\left((V_{(i,u)}^{dc}-V_{(i,n)}^{dc})-(V_{(i,w)}^{dc}-V_{(i,n)}^{dc})\right) \tag{32b}$$

The common-mode current of a DC DG is calculated from (33a), as a function of the common-mode voltage (see (33b)) and the common mode admittance of DG.

$$I_{com(i)}^{dc}=V_{com(i)}^{dc}\cdot Y_{com(i)}^{dc} \tag{33a}$$

$$V_{com(i)}^{dc}=\frac{1}{2}\cdot\left((V_{(i,u)}^{dc}-V_{(i,n)}^{dc})+(V_{(i,w)}^{dc}-V_{(i,n)}^{dc})\right) \tag{33b}$$

The currents $I_{(i,u)}^{dc}$, $I_{(i,w)}^{dc}$ in (23) are written as a function of sequence components above as follows:

$$I_{(i,u)}^{dc}=I_{diff\,(i)}^{dc}+I_{com(i)}^{dc} \tag{34a}$$

$$I_{(i,w)}^{dc}=-I_{diff\,(i)}^{dc}+I_{com(i)}^{dc} \tag{34b}$$

Equation (35a) expresses the currents of DG bus i in the form that are included in $\boldsymbol{I_{new}^{dc}}$ of (27). Thus, $\boldsymbol{Y_{DG}^{dc}}$ in (35b) can be transferred to the right side of (27) providing an implicit representation of common-mode sequence component into the $\boldsymbol{Y_{new}^{dc}}$ matrix. The common mode admittance in (35b) is determined based on the control mode of DC-DG as follows:

i. $Y_{com(i)}^{dc}\to\infty$ for two-poles-to-neutral DGs with balanced pole-to-neutral voltage.

ii. $Y_{com(i)}^{dc}\to 0$ for two-poles-to-neutral DGs with balanced current.

$$\begin{bmatrix} I_{(i,u)}^{dc} \\ I_{(i,w)}^{dc} \\ -I_{(i,u)}^{dc}-I_{(i,w)}^{dc} \\ 0 \end{bmatrix}=\begin{bmatrix} I_{diff\,(i)}^{dc} \\ -I_{diff\,(i)}^{dc} \\ 0 \\ 0 \end{bmatrix}+\boldsymbol{Y_{DG}^{dc}}\cdot\begin{bmatrix} V_{(i,u)}^{dc} \\ V_{(i,w)}^{dc} \\ V_{(i,n)}^{dc} \\ V_{(i,g)}^{dc} \end{bmatrix} \tag{35a}$$

$$\boldsymbol{Y_{DG}^{dc}}=\frac{1}{2}\cdot\begin{bmatrix} Y_{com(i)}^{dc} & Y_{com(i)}^{dc} & -2\cdot Y_{com(i)}^{dc} & 0 \\ Y_{com(i)}^{dc} & Y_{com(i)}^{dc} & -2\cdot Y_{com(i)}^{dc} & 0 \\ -2\cdot Y_{com(i)}^{dc} & -2\cdot Y_{com(i)}^{dc} & 4\cdot Y_{com(i)}^{dc} & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{35b}$$

IV. Interlinking Converter

Usually, the active power of ICs is determined based on the level of loading (LoL) of two subgrids. The level of loading of AC and DC subgrids is estimated as follows in (36) and (37), respectively [6]:

$$f_{LoL}=\frac{f-0.5\cdot(f_{max}+f_{min})}{0.5\cdot(f_{max}-f_{min})} \tag{36}$$

$$V_{LoL}^{dc}=\frac{V_{IC}^{dc}-0.5\cdot(V_{IC,\max}^{dc}+V_{IC,\min}^{dc})}{0.5\cdot(V_{IC,\max}^{dc}-V_{IC,\min}^{dc})} \tag{37}$$

The parameters f_{LoL}, f, f_{max}, and f_{min} of the above equations denote the LoL (f_{LoL}), the actual (f), the maximum (f_{max}), and minimum (f_{min}) frequency of the AC subgrid, respectively. The parameters V_{LoL}^{dc}, V_{IC}^{dc}, $V_{IC,max}^{dc}$, $V_{IC,min}^{dc}$ denote the LoL (V_{LoL}^{dc}), the actual differential mode voltage (V_{IC}^{dc}), the maximum ($V_{IC,max}^{dc}$) and minimum ($V_{IC,min}^{dc}$) differential mode voltage of DC side of IC, respectively. Below, two of the most common control modes of ICs are described.

1. Droop Controlled IC

The difference between the LoL of two subgrids is denoted as $\Delta e=f_{LoL}-V_{LoL}^{dc}$. The power flowing through the IC is determined based on Δe of the last iteration k and the droop parameter $K_{P(i)}^{IC}$, as shown in (38) [6], [10]:

$$P_{ic}^{\,k+1}=\frac{1}{K_{P(i)}^{IC}}\cdot\Delta e^k \tag{38}$$

A positive value of Δe indicates that the AC subgrid is less loaded than the DC subgrid and therefore the IC is forced to transfer active power from the AC to DC subgrid.

Thus, P_{ic} is set positive in the AC subgrid (consumption mode) and negative in the DC subgrid (generation mode). The opposite occurs when $\Delta e < 0$.

2. PI controlled IC

Scope of the second control strategy is to nullify the value of Δe so that both subgrids achieve the same LoL [7], [9]. In this control mode, the IC active power is calculated according to (39):

$$P_{ic}^{k+1} = P_{ic}^{k} + c \cdot \Delta e^{k} \tag{39}$$

where c is a suitably selected gain and k is the iteration number. Applying (39), after a number of iterations Δe is forced to zero and the two subgrids achieve the same LoL.

V. Unified Algorithm for Islanded HMGs

In this section, a unified power flow algorithm is presented aiming to unify in one matrix the AC and DC subgrids of an HMG. More specifically, by combining (13) and (28), (40) is derived to model HMGs.

$$\begin{bmatrix} \boldsymbol{Y}_{fin2}^{ac} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{Y}_{fin2}^{dc} \end{bmatrix}^{-1} \cdot \left(\begin{bmatrix} \boldsymbol{I}_{new}^{ac} - \boldsymbol{Y}_{fin1}^{ac} \cdot \boldsymbol{V}_{0}^{ac} \\ \boldsymbol{I}_{new}^{dc} - \boldsymbol{Y}_{fin1}^{dc} \cdot \boldsymbol{V}_{0}^{dc} \end{bmatrix} \right)^{k} = \begin{bmatrix} \boldsymbol{V}_{fin}^{ac} \\ \boldsymbol{V}_{fin}^{dc} \end{bmatrix}^{k+1} \tag{40}$$

The IC buses of AC and DC subgrids (buses connected with IC) are treated as load or generator buses. The IC power is estimated from (38) or (39) depending on the adopted control mode. The solution process of the proposed algorithm consists of the following steps:

1. The AC and DC admittance matrices are modified to incorporate the matrices of (19b) and (35b) respectively. Thus, the negative-, zero- and common-mode-sequence components of DGs are implicitly considered in the Y_{BUS} admittance matrices of both subgrids, enhancing the convergence speed and robustness of the algorithm.
2. The frequency of AC subgrid is updated from (14) so that the power flowing through the virtual AC slack bus (calculated in (3)) is nullified.
3. Both AC and DC virtual slack buses are equalized with their adjacent buses according to (4) and (22).
4. The AC matrices $\boldsymbol{Y}_{fin1}^{ac}$, $\boldsymbol{Y}_{fin2}^{ac}$ are updated based on the new frequency, as calculated in Step 2.
5. The active and reactive power of ICs and DGs are estimated from their droop equations, based on the last voltage and frequency values.
6. The matrices $\boldsymbol{I}_{new}^{ac}$ and $\boldsymbol{I}_{new}^{dc}$ are updated.
7. Eq. (40) is applied to calculate the new network voltages.
8. If the difference between the voltages of two consecutive iterations is less than a predefined tolerance ε, the algorithm terminates. Otherwise, it moves back to Step 2.

VI. Algorithm Validation

The results of the proposed approach are validated in this section against the results of Simulink and the method of [13] in a 12-Bus and a 47-Bus hybrid AC/DC islanded network, respectively.

A) 6-Bus AC/6-Bus DC Network

To the best of our knowledge, all the existing power flow methods of HMGs examine only unipolar DC subgrids and 1- or 3-wire AC subgrids. There is not a method so far, to examine bipolar DC and 4-wire multigrounded AC subgrids. Thus, the validation of the proposed approach should be necessarily realized against time-domain software. Due to the time consuming nature of the time-domain softwares, a sufficiently small network of 12-Bus was selected, as shown in Fig. 3. It consists of a 6-Bus 4-wire multigrounded AC network connected through an IC with a 6-Bus bipolar DC network. The loads and parameters of both subgrids are presented in Tables I and II.

The results of AC and DC subgrids are depicted in Tables III and IV, respectively. As shown, all the results of the proposed algorithm are in full agreement with them of Simulink. It is pointed out, that the IC was set to transfer 10 kW of constant active power from AC to DC subgrid. The reactive power at the AC side of IC is considered equal to zero. The AC side of IC generates balanced current, while the DC side balanced pole-to-neutral voltage. All AC and DC DGs are assigned to generate balanced phase- or pole-to-neutral voltages. Nevertheless, the execution time of the proposed approach is highly reduced compared to Simulink from several minutes to less than 10ms for a voltage accuracy of 10^{-6} V.

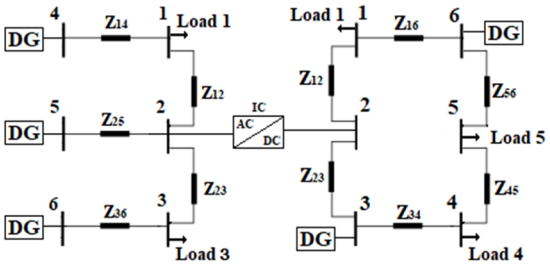

Fig. 3. Islanded 12-Bus HMG [10].

TABLE I
Parameters of Unbalanced 6-Bus AC Subgrid

Resistance of the lines	0.5 Ohm/km
Self-Reactance of the lines	0.6 mH/km
Mutual-Reactance of the lines	0.1 mH/km
Line lengths	0.1 km
Loads of PQ buses	See Table III
$\boldsymbol{K_{P(i)}^{ac}}$ **(i=4, 5, 6)**	$5 \cdot 10^{-6}$ (Hz/W)
$\boldsymbol{K_{Q(i)}^{ac}}$ **(i=4, 5, 6)**	$2 \cdot 10^{-4}$ (V/VAR)
$\boldsymbol{V_{ref(i)}^{ac}}$ **(i=4, 5, 6)**	230 V
$\boldsymbol{f_{ref(i)}}$ **(i=4, 5, 6)**	50 Hz
Ground resistances	25 Ohm
$(\boldsymbol{P_{max}}, \boldsymbol{S_{max}})$ **of DGs**	(15kW, 20kVA)
$(\boldsymbol{P_{max}}, \boldsymbol{S_{max}})$ **of IC**	(10kW, 10kVA)
Nominal phase-to-neutral voltage of the network	230 V

TABLE II
Parameters of Unbalanced 6-Bus DC Subgrid

Resistance of the lines	4.7 Ohm/km [6]
Line lengths	0.1 km
Loads of P buses	See table IV
$\boldsymbol{V_{ref(i)}^{dc}}$ **(i=3, 6)**	230 V
$\boldsymbol{K_{P(i)}^{dc}}$ **(i=3, 6)**	$5 \cdot 10^{-4}$ (V/W)
$\boldsymbol{P_{max}}$ **of DGs**	10 kW
Nominal pole-to-neutral voltage of the network	230 V

TABLE III
COMPARATIVE RESULTS FOR THE ISLANDED 6-BUS AC SUBGRID

Bus - Phase	Phase-to-neutral Voltage (V)		Active Power (kW)		Reactive Power (kVar)	
	Proposed	Simulink	Proposed	Simulink	Proposed	Simulink
1a	227.3415	227.3414	5	5	3.75	3.75
1b	227.6681	227.6680	4	4	3	3
1c	228.3640	228.3641	3	3	2.25	2.25
2a	227.6050	227.6051	3.328	3.328	0.0034	0.0034
2b	227.8231	227.8231	3.333	3.333	-0.0034	-0.0034
2c	228.2869	228.2869	3.339	3.339	0	0
3a	227.3415	227.3414	5	5	3.75	3.75
3b	227.6681	227.6681	4	4	3	3
3c	228.3640	228.3641	3	3	2.25	2.25
4a	228.7624	228.7624	-4.561	-4.561	-2.626	-2.626
4b	228.7624	228.7624	-3.794	-3.794	-2.068	-2.068
4c	228.7624	228.7624	-3.036	-3.036	-1.493	-1.493
5a	228.8642	228.8642	-4.307	-4.307	-2.268	-2.268
5b	228.8642	228.8642	-3.795	-3.795	-1.896	-1.896
5c	228.8642	228.8642	-3.289	-3.289	-1.513	-1.513
6a	228.7624	228.7624	-4.561	-4.561	-2.626	-2.626
6b	228.7624	228.7624	-3.794	-3.794	-2.068	-2.068
6c	228.7624	228.7624	-3.036	-3.036	-1.493	-1.493
MG frequency: Proposed: f = 49.9430 Hz Simulink: f = 49.9430 Hz						

TABLE IV
COMPARATIVE RESULTS FOR THE ISLANDED 6-BUS DC SUBGRID

Bus - Phase	Pole-to-neutral Voltage (V)		Active power (kW)	
	Proposed	Simulink	Proposed	Simulink
1u	229.8357	229.8357	2	2
1w	-228.2501	-228.2501	2.5	2.5
2u	234.4040	234.4040	-4.87	-4.87
2w	-234.4040	-234.4040	-5.13	-5.13
3u	229.7397	229.7397	0.012	0.012
3w	-229.7397	-229.7397	-0.532	-0.532
4u	226.2067	226.2067	2	2
4w	-222.8792	-222.8792	2.5	2.5
5u	225.7249	225.7249	2	2
5w	-222.3948	-222.3948	2.5	2.5
6u	228.3006	228.3006	-1.30	-1.30
6w	-228.3006	-228.3006	-2.09	-2.09

B) 25-Bus AC/22-Bus DC Network

To further validate the proposed algorithm, we compare it against the method of [13] in a 47-Bus hybrid AC/DC islanded MG. The network configuration is depicted in Fig. 4. It consists of a 3-wire AC unbalanced network connected through two ICs with a unipolar DC network. Four DC DGs are connected in the DC network and three AC DGs are connected in the AC network operating in different modes. Data about the DGs and ICs are provided in Tables V, VI and VII in per unit. Data about the loads and lines are not included in the manuscript due to space limitation but they are provided in [13]. The base power and voltage of the AC and DC subgrids are: $S_{base-3ph} = 5\ MVA$, $V_{base-LL} = 4.16\ kV$, $P_{base-dc} = 5\ MW$, $V_{base-dc} = 15\ kV$.

The results of the proposed approach are in full agreement with them of [13, Table IX] although they are not depicted in the manuscript due to space restriction. It is noted that the transformer of the investigated topology was simulated using the transformer model of [18, Table IV]. A detailed analysis of transformer modeling is provided in [18] and it is out of the scope of this paper.

TABLE V
AC DGS RATINGS AND DROOP SETTINGS (IN PU) FOR THE 47-BUS HMG

Buses	$K^{ac}_{P(i)}$	$K^{ac}_{Q(i)}$	$V^{ac}_{ref(i)}$	$f_{ref(i)}$	$P^{max}_{G,ac}$	$S^{max}_{G,ac}$
1	0.0397	0.1323	1.01	1.00833	0.504	0.630
4	0.0556	0.1852	1.01	1.00833	0.360	0.450
16'	0.0500	0.1667	1.01	1.00833	0.400	0.500

TABLE VI
DC DGS RATINGS AND DROOP SETTINGS (IN PU) FOR THE 47-BUS HMG

Buses	$K^{dc}_{P(i)}$	$V^{dc}_{ref(i)}$	$P^{max}_{G,ac}$
4 & 13	0.5	1.05	0.2
8 & 15	0.4	1.05	0.25

TABLE VII
IC RATINGS AND DROOP SETTINGS (IN PU) FOR THE 47-BUS HMG

IC	$K^{IC}_{P(i)}$	$K^{IC}_{Q(i)}$	$V^{IC}_{ref(i)}$	$V^{dc}_{IC,max}$	$V^{dc}_{IC,min}$	f_{max}	f_{min}	S^{IC}_{max}
#1	30	1	1.01	1.0047	0.9953	1.0047	0.9953	0.1
#2	60	2	1.01	1.0047	0.9953	1.0047	0.9953	0.05

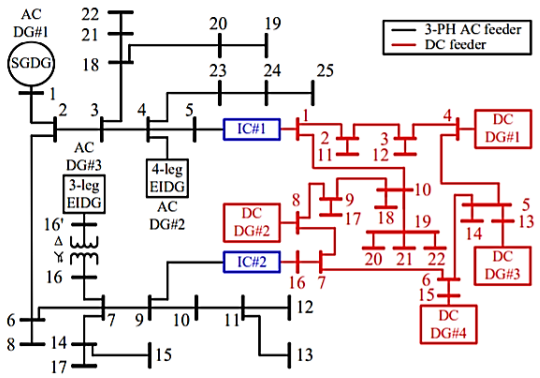

Fig. 4. Islanded 47-Bus HMG [13].

VII. ALGORITHM PERFORMANCE

The performance of the proposed approach with respect to computation time and robustness is investigated below.

A) Computation Time

The computation time of the proposed approach is compared against several existing power flow methods for islanded AC and hybrid AC/DC MGs. For the sake of fairness all simulations were executed in a PC 64-bit Intel Core i7, 3.4GHz CPU with 16GB RAM. The execution time of each method for a voltage accuracy of 10^{-6} (pu) is depicted in Table VIII showing that the proposed approach presents by far the best computational performance for both AC and hybrid AC/DC islanded MGs. It is pointed out that the fundamental difference between the proposed method and the method of [11] lies in the modeling of DGs. In the proposed method, the negative- and zero-sequence current of DGs are implicitly introduced in Y_{BUS} matrix through the (19b) and (35b), while in [11] the DG currents are explicitly considered through [11, eq. (17)] and [11, eq. (18)]. This modification greatly reduces the iteration number and therefore the computation time of the algorithm.

TABLE VIII
COMPARISON OF COMPUTATION TIME

	Execution time	
	Hybrid 25-Bus AC/22-Bus DC Islanded Network	25-Bus AC Islanded Network
Proposed Method	34 ms	26 ms
NR [13][19]	162.5 ms [13]	75 ms [19]
NTR [12]	3800 ms [12]	3220 ms [19]
Method of [11]	Not applicable	180 ms

B) Computation Robustness

Authors in [15] deduced that implicit Z_{BUS} method is inevitably convergent as far as a power flow solution exists. The proposed approach is a modified version of implicit Z_{BUS} method, thus it takes advantage of its excellent robustness. In this sub-section, the robustness of the proposed algorithm for a wide range of conditions e.g initial voltage values, *R*/*X* line ratio, loading of the MG is tested using the 47-Bus network of Fig. 4.

Firstly, the convergence speed of the algorithm for a wide range of initial AC and DC voltage values between 0.3 to 2 pu is depicted in Fig. 5a. As shown, the algorithm achieves convergence for all the range of initial voltage values. Secondly, the convergence speed of the algorithm for several *R*/*X* ratios (from 0.1 to 20) is shown in Fig. 5b, while in all cases the impedance magnitude is kept constant. The algorithm converges for all the range of *R*/*X* ratios enabling its applicability in all kind of networks, from high-resistive LV to low-resistive HV networks.

Thirdly, the load of each node (for both subgrids) is multiplied by a factor λ ranging from 0.2 to 2.1. The convergence rate of the algorithm is shown in Fig. 5c. The convergence rate is constant for all the loading factors up to λ=1.8. For λ>1,82 the active power limit of all AC DGs is reached and any additional active power rise is completely covered by the ICs. For λ>2.03 the ICs power limit is also reached and any additional active power rise of AC loads cannot be covered. As a result, the power flow problem does not have a solution. This is the reason for the algorithm divergence for λ>2,03.

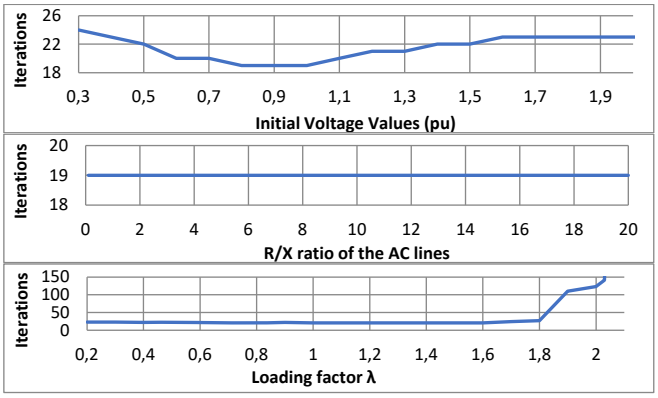

Fig. 5. From top to bottom: a) Iteration number for several initial voltage values, b) Iteration number for several *R*/*X* line ratios, c) Iteration number for several values of λ. The voltage accuracy in all cases is 10^{-6} pu.

VIII. Implementation on a Large-Scale Network

In this Section, the performance of the proposed power flow algorithm is evaluated on a large-scale AC/DC microgrid under unbalanced loading conditions. The topology of the examined network is depicted in Fig. 6, consisting of two subgrids, i.e., the AC and the DC subgrid. The former is a modified version of the IEEE 906-Bus European LV test feeder [20], while the latter is a fictitious 118-Bus bipolar DC grid. The topology of the DC subgrid is obtained from [21]. These two subgrids are connected through an IC with a nominal power equal to 60 kVA.

In the next subsections, the configuration of the system under study is analytically presented followed by a comparative analysis between the proposed algorithm and the NR and NTR solutions presented in the literature.

A) Network Configuration

Considering the AC subgrid, the nominal frequency and the phase-to-phase voltage are equal to 50 Hz and 416 V, respectively. Furthermore, the nominal pole-to-neutral voltage of the DC subgrid is 380 V, which is a reliable, cost-effective and efficient voltage level for commercial DC installations [22]. Both subgrids are interconnected through an IC between the AC bus 817 and the DC bus 1, as shown in Fig. 6. The parameters of both subgrids are analytically described below:

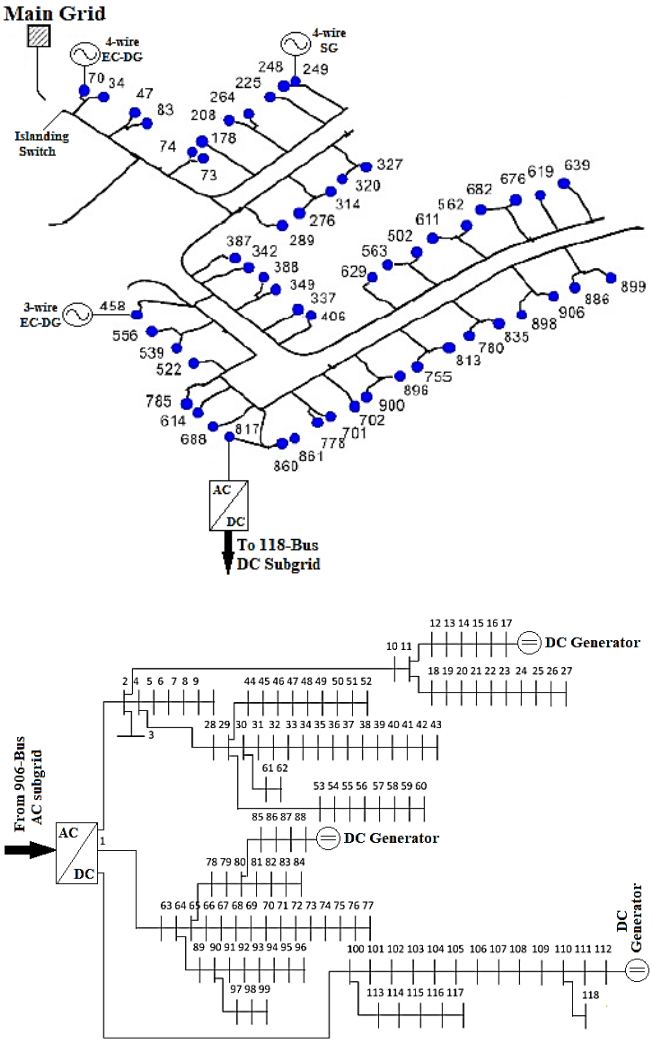

Fig. 6. Single-line diagram of the examined AC/DC unbalanced microgrid. From top to bottom: a) three-phase AC subgrid and b) bipolar DC subgrid.

1) *Generation and IC Modeling*

According to Fig. 6a, the AC subgrid includes three DG units operating in droop control mode as follows: a) a 4-wire EC-DG is connected to bus 70 that generates balanced phase-to-neutral voltages, b) a 4-wire SG unit is connected to bus 249, and c) a 3-wire EC-DG is connected to bus 458 generating balanced current.

On the other hand, the DC subgrid includes three DG units connected to the buses 17, 88, 112 as shown in Fig. 6b. All DC DGs generate balanced pole-to-neutral voltages. Finally, the IC operates in PI control mode. The AC-side of IC generates balanced currents, while the DC-side forms balanced pole-to-neutral voltages. The control parameters of the IC as well as the droop parameters of the DG units are given in Table IX.

TABLE IX
PARAMETERS OF DGS AND IC

AC DGs: $K^{ac}_{P(i)}$ (i=70, 249, 458)	$1 \cdot 10^{-6}$ (Hz/W)
AC DGs: $K^{ac}_{Q(i)}$ (i=70, 249, 458)	$2 \cdot 10^{-4}$ (V/VAR)
AC DGs: $V^{ac}_{ref(i)}$ (i=70, 249, 458)	245 V
AC DGs: $f_{ref(i)}$ (i=70, 249, 458)	50 Hz
AC DGs: P_{max}, S_{max}	250 kW, 300 kVA
SG-DG: Y_0 (see eq. (19b))	2.5 – 2.5·j
SG-DG: Y_2 (see eq. (19b))	2.5 – 2.5·j
DC DGs: $V^{dc}_{ref(i)}$ (i=17, 88, 112)	380 (V)
DC DGs: $K^{dc}_{P(i)}$ (i=17, 88, 112)	$2.5 \cdot 10^{-4}$ (V/W)
DC DGs: P_{max}	100 kW
IC: f_{min}, f_{max}	49.5 Hz – 50.5 Hz
IC: $V^{dc}_{IC,min}$, $V^{dc}_{IC,max}$	280V, 480V
IC: Reactive power	0 kVar
IC: Gain c (see eq. (39))	$2 \cdot 10^{5}$
IC: S_{max}	60 kVA

2) *Consumption Modeling*

The loads of the AC subgrid are increased to investigate the behavior of the proposed algorithm under highly loaded conditions. More specifically, every bus depicted with a blue dot in Fig. 6a supplies an unbalanced three-phase load with a power equal to (P_a, P_b, P_c) =(1.5kW, 2kW, 2.5kW). Thus, the total loading of phases *a*, *b* and *c* is 82.5kW, 110kW and 137.5kW, respectively. Note that all the AC loads operate with an inductive power factor of 0.95 [20].

The 118-Bus DC subgrid supplies in total 236 loads, i.e. two loads for each bus, connected between one pole and neutral. At each bus, the pole *u* supplies a load of 0.7kW, while the pole *w* 1kW. Therefore, the pole *u* supplies a total load of 82.6kW, while the pole *w* 118kW.

3) *Lines and Grounding*

The impedance of the lines of the IEEE 906-Bus European LV test network is given in the form of sequence impedance Z_0, Z_1, Z_2. Thus, a conversion of the impedance matrix of each line from the sequence components to the a-b-c-n-g representation is necessary. This is attained by introducing the following assumptions for each AC line:

- Equal self-impedance of the phases/neutral.
- Equal mutual-impedances among phases/neutral.
- Zero mutual-impedances between ground and the phases/neutral.
- Zero self-impedance of the ground.

The EC-DGs connected to the AC buses 70 and 249 are solidly grounded with a resistance equal to 0.1 Ωhm. Moreover, the buses with loads are grounded with a resistance of 25 Ωhm, which is a typical value for household installations. The remaining buses are ungrounded.

The resistance of all DC lines is 0.668 Ohm/km and the distance between two successive buses is 50m. The neutral of DC DG units and the neutral of DC side of IC are solidly grounded with a resistance 0.1 Ohm [23], while all the other buses are ungrounded.

B. Numerical Results of the AC Subgrid

The proposed power flow algorithm is compared against the sequence component NR [13] and NTR [12] power flow approaches. It is noted that the NR [13] and NTR [12] methods produce identical results since they are based on the same assumption of a perfectly grounded neutral.

In Fig. 7, the deviation of the phase-to-neutral voltages for each node between the proposed algorithm and the NR/NTR methods is depicted. It can be observed that significant deviations up to 4 V exist between the proposed approach and the existing methods especially for the less loaded phase A and the most loaded phase *C*.

Moreover, the NR and NTR methods underestimate the active and reactive power losses of the network due to the assumption of a perfectly grounded neutral, thus neglecting the corresponding losses. More specifically, as shown in Fig. 8, the active and reactive losses calculated by the proposed approach is 18.98 kW and 3.36 kVar, respectively, while the losses estimated by the NR/NTR methods are 18.02 kW and 2.97 kVar. The deviation is about 5 % for the active power and 12 % for the reactive power.

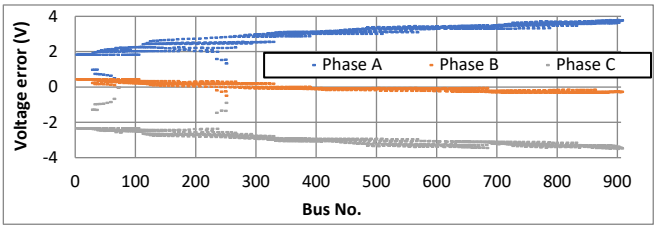

Fig. 7. Voltage deviation of phase-to-neutral voltage between the proposed and the NR/NTR power flow methods.

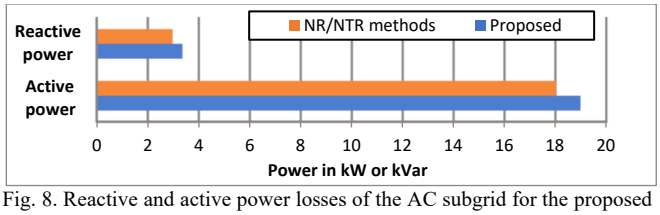

Fig. 8. Reactive and active power losses of the AC subgrid for the proposed and the NR/ NTR algorithms.

Fig. 9 depicts the neutral-to-ground voltage profile, which is known as ground potential rise (GPR), of the investigated AC subgrid using the proposed method and the NR/NTR methods. As shown, the proposed method enables the calculation of GPR, which in some buses of the investigated network takes large values, more than 7 V. On the contrary, NR and NTR methods ignore the GPR due to the assumption of a perfectly grounded neutral.

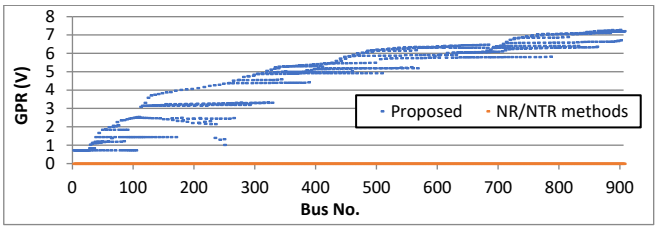

Fig. 9. Ground potential rise of the AC subgrid for the proposed algorithm and the NR/NTR methods.

The voltage stability is a very important analysis tool in power systems. It indicates the maximum load that the network can support, beyond which it collapses [24]. This maximum load is referred as maximum loadability of the network. Lately, the study of the maximum loadability in islanded MGs has gained the interest of several research groups [24]-[26]. The estimation of voltage stability requires an accurate and robust power flow solver that achieves convergence near the ill-conditioned stability limit.

To estimate the maximum loadability of the AC subgrid, the base loads of all the AC nodes (given in Section

VIII.A.2) are multiplied by a stepwise increasing factor λ, while the DC loads remain constant. Due to their large power capacity, the power limits of AC DGs are not reached for any examined value of λ. Fig. 10a illustrates the phase-to-neutral voltage of the less and most loaded phase A and C, respectively, as a function of λ for the bus 899. Fig. 10b depicts the GPR of the same bus for the same range of λ. Three observations are made based on Fig. 10: a) The proposed approach is robust enough since it achieves convergence near the voltage stability limit; b) the NR/NTR present considerable inaccuracies compared to the proposed method, due to the assumption of a perfectly grounded neutral; c) the GPR, which takes dangerous values as the loadability increases, can be calculated only by the proposed approach.

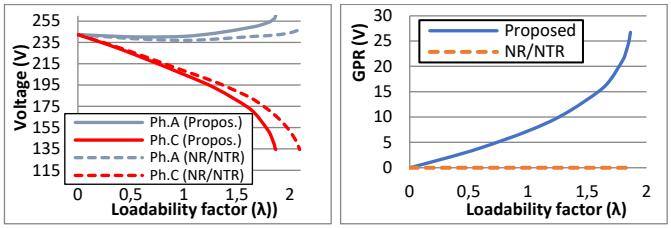

Fig. 10. From left to right: a) voltage stability curve of phases A, C of the bus 899, and b) ground potential rise for the same bus.

C. Numerical Results of the DC Subgrid

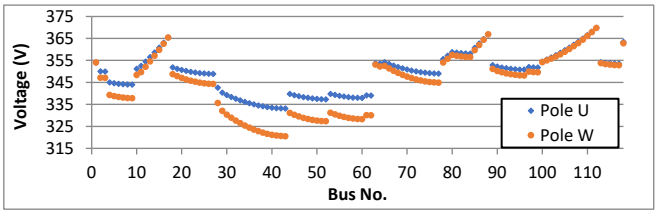

Fig. 11. Pole-to-neutral voltage for the 118-Bus DC subgrid.

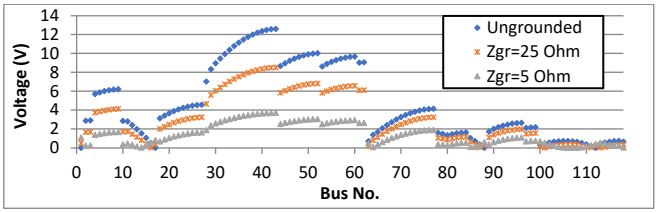

Fig. 12. Neutral-to-ground voltage for the 118-Bus DC subgrid, considering different grounding resistances.

Fig. 11 depicts the pole-to-neutral voltages of the 118-Bus DC subgrid. Please note, that all the power flow approaches proposed in literature so far consider a unipolar DC subgrid, thus a comparison with them cannot be made. Therefore, only some indicative results of the proposed method will be presented. As shown, due to the unbalanced loading between the poles, the voltage of some remote buses (e.g bus 43) is highly unbalanced. On the other hand, the buses near the IC and DGs are not affected too much from the unbalances due to the voltage balancing that DGs and IC provide.

Fig. 12 illustrates the GPR of the 118-Bus DC subgrid for three different cases: a) all load buses remain ungrounded; b) all load buses are grounded with a grounding resistance 25 Ωhm; and, c) with a grounding resistance 5 Ωhm. In all cases DGs and IC are solidly grounded with a resistance 0.1 Ωhm. As shown, in all cases the IC and DGs have a negligible GPR because of the solid grounding. On the other hand, an increased GPR is observed in the remote buses depending on the grounding resistances. Low grounding resistances reduce the GPR but increase the stray currents, which in DC networks cause a serious corrosion in buried metallic infrastructure [27]. It is obvious that the study of these effects requires an accurate power flow solver, like the one presented in this paper.

D. Numerical Results of the IC

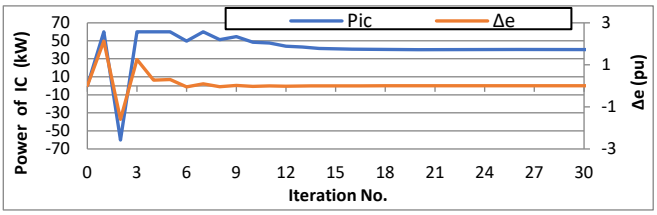

Fig. 13. Active power of IC (left vertical axis) and Δe (right vertical axis) as a function of the iteration number.

The active power of the IC and the difference of the level of loading (LoL) of two subgrids (Δe) are depicted in Fig. 13, during the iterative power flow process. It is noted that a positive value of active power means power transmission from AC to DC subgrid. It is also clarified that during the iterative process, a limiter at ±60kW was set to the power of IC, in order to prevent it from converging to a value higher than the maximum IC power. As shown, the power converges to 40.15kW and the Δe to zero with an accuracy of 10^{-6}, after 30 iterations, confirming the flexibility to treat different IC control modes.

E. Computational Burden

The computation time of the power flow of the 906-Bus AC/ 118-Bus DC islanded network is 1.05 sec, assuming a voltage accuracy of 10^{-6} pu. This time is very low given the large size of the network. For comparison, the NR [12] and NTR [13] methods spend 1.15 sec and 91.96 sec for solving the power flow of a much smaller 123-Bus AC/22-Bus DC network, according to [13, Table XIII].

It is noted that in the proposed algorithm, the inductances of the lines are calculated assuming a constant frequency and they are not updated during the iterative process. Thus, the step 4 of Section V, which is the most time-consuming step due to the inversion of the large matrix $\boldsymbol{Y}_{fin2}^{ac}$, is avoided. The inaccuracy caused by the consideration of a constant inductance is negligible since the frequency in islanding should vary in the small range between 49 Hz and 51 Hz, according to the standard EN 50160. For instance, in the investigated network, the frequency is 49.87 Hz.

In the case that the frequency has a large variation, several matrices $\boldsymbol{Y}_{fin2}^{ac}$ can be calculated and saved offline, each of which corresponds to a small specified frequency range. They are selected in every iteration depending on the calculated frequency. In this way the most time-consuming action of the matrix update and inversion is avoided and the computation time is extremely low. On the other hand, in NR-based methods, the update and inversion of Jacobian matrix cannot be avoided since it is a fundamental part of the algorithm. Thus, in large networks with large Jacobian matrices, the computation time is significantly higher.

TABLE X
OVERALL COMPARISON BETWEEN POWER-FLOW APPROACHES FOR HYBRID AC/DC MICROGRIDS [13]

	Balanced NTR [6]	Unified NR [10]	GRG [7]	Sequential NR [9]	BFS [8]	Unbalanced NTR [12]	NR-Sequence Components [13]	Proposed Approach
Algorithm/Formulation	Unified	Unified	Unified	Sequential	Sequential	Unified	Sequential	Unified
Computational Cost	High	High	High	Low	Low	High	Low	Very Low
Droop-Controlled AC-DG Types/Models	Balanced DGs	Balanced DGs	Balanced DGs	Balanced DGs	Balanced DGs	Balanced DGs	SGDG, 4-Leg and 3-Leg EIDG	SGDG, 4-Leg and 3-Leg EIDG
Solves Unbalanced AC Subgrids	No	No	No	No	No	Yes (abc frame)	Yes (012 frame)	Yes (abcng frame)
Incorporates Delta Loads	No	No	No	No	No	No	Yes	Yes
Transformer Connections	No	No	No	No	No	No	Yes	Yes
SVR Modeling	No	No	No	No	No	No	Not referred	Yes [28]
Solves Bipolar DC	No	No	No	No	No	No	Not referred	Yes
Explicit Representation of Neutral-Grounding	No	No	No	No	No	No	No	Yes
Incorporation of Virtual Impedance Control of DGs	No	No	No	No	No	No	Not referred	Yes [11]

IX. CONCLUSION

In this paper, a precise power flow algorithm for unbalanced islanded HMGs is presented considering the neutral and grounding of both AC and bipolar DC subgrids. To the authors' knowledge, this is the first time that such a precise model is presented in literature for solving the power flow in islanded HMGs considering also the asymmetries of subgrids. The algorithm presents very low computation time making it a useful tool for real-time network estimation and optimization applications. It is generic since it can be applied to all network configurations (meshed and radial) and operation modes (grid-connected and islanded). Furthermore, a comprehensive modeling of DGs is proposed, which greatly enhances the convergence speed and robustness compared to the DG modeling adopted in [11]. Simulations results showed that the proposed algorithm produces more precise results than the other existing algorithms, while the computation time is significantly lower. A summary of the main advantageous characteristics of the proposed approach compared with other existing methods is provided in Table X.

APPENDIX

A case study of a large scale multi-terminal hybrid 2520-Bus AC/118-Bus DC network is provided as supplementary material of this paper.

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Supplementary Material

I. Introduction

This report presents some simulation results of the proposed power flow approach on a large scale hybrid 2520AC/118DC unbalanced islanded microgrid (MG).

II. Network Description and Simulation Results

The AC subgrid is based on the IEEE 8500-Nodes test feeder shown in Fig. 1a [1], [2], while the DC subgrid is a fictitious 118-bus bipolar DC subgrid depicted in Fig. 1b. These two subgrids are connected through three 60kVA ICs, forming this way a multi-terminal hybrid AC/DC grid.

A) Network Configuration

The original IEEE 8500-Node test feeder consists of 8500 node points, which correspond to 4800 1-, 2-, and 3-phase bus locations [1], [2]. Among the 4800 Buses, 2520 of them are primary MV buses, while the remaining are secondary LV buses. The MV network is a 4-wire network, which use the neutral to distribute the power to the secondary LV buses [2].

In this report, we consider only the 2520 MV buses, while the LV buses are simply modeled as constant loads. The nominal frequency and phase-to-neutral voltage of the AC network is 50 Hz and 7.2 kV, respectively. The network includes 4 step voltage regulators (SVRs) and capacitors, as shown in Fig. 1a. The pole-to-neutral voltage of the DC subgrid is 380 V. The subgrids are interconnected through 3 ICs connecting the following (AC-DC) buses: (817-1), (800-27), (750-43). The parameters of both subgrids are described below in more details.

1) *DGs and ICs*

The AC subgrid consists of 4 AC DGs operating in droop-control as follows: a) a 4-wire EC-DG is connected to bus 70 that generates balanced phase-to-neutral voltage, b) a 4-wire SG is connected to bus 249, c) a 3-wire EC-DG is connected to bus 458 generating balanced currents, d) a 3-wire EC-DG is connected to bus 1500 that generates balanced phase-to-phase voltage.

The DC subgrid includes three DG units connected to buses 17, 88, 112, as shown in Fig. 1b. All DC DGs generate balanced pole-to-neutral voltages. Finally, the ICs operate in droop-control mode. The AC side of ICs generates balanced currents, while the DC side forms a balanced pole-to-neutral voltage. The control parameters of DGs and ICs are given in Table I.

2) *Loads*

The loads of the AC subgrid are given in [2]. The total loading of the network is 10.77 MW. The power factor of each load is inductive and equal to 0.97. The 118-Bus DC subgrid supplies in total 236 loads, i.e. two loads for each bus, connected between one pole and neutral. At each bus, the pole *u* supplies a load of 0.7kW, while the pole *w* 1kW. Therefore, the pole *u* supplies a total load of 82.6kW, while the pole *w* 118kW.

3) *Lines and Grounding*

The line impedances of the AC subgrid are given in [2]. Although some lines of the IEEE 8500-Node test feeder consists of 1- and 2-phase lines, we simulate them as 3-phase lines in order to facilitate the construction and treatment of the Y_{BUS} matrix as well as to facilitate the interpretation of the results. This consideration does not influence the results at all since the current flown through the added lines is zero.

The 4-wire DGs connected to AC buses 70 and 249 are solidly grounded with a resistance equal to 0.1 Ω. Moreover, the AC buses with loads are grounded with a resistance of 25 Ω, unless otherwise stated.

Regarding the DC network, the resistance of all DC lines is 0.668 Ohm/km and the distance between two successive buses is 50m. The neutral of the DC DG units and the neutral of the DC side of ICs are solidly grounded with a resistance 0.1 Ohm, while all the other DC buses remain ungrounded.

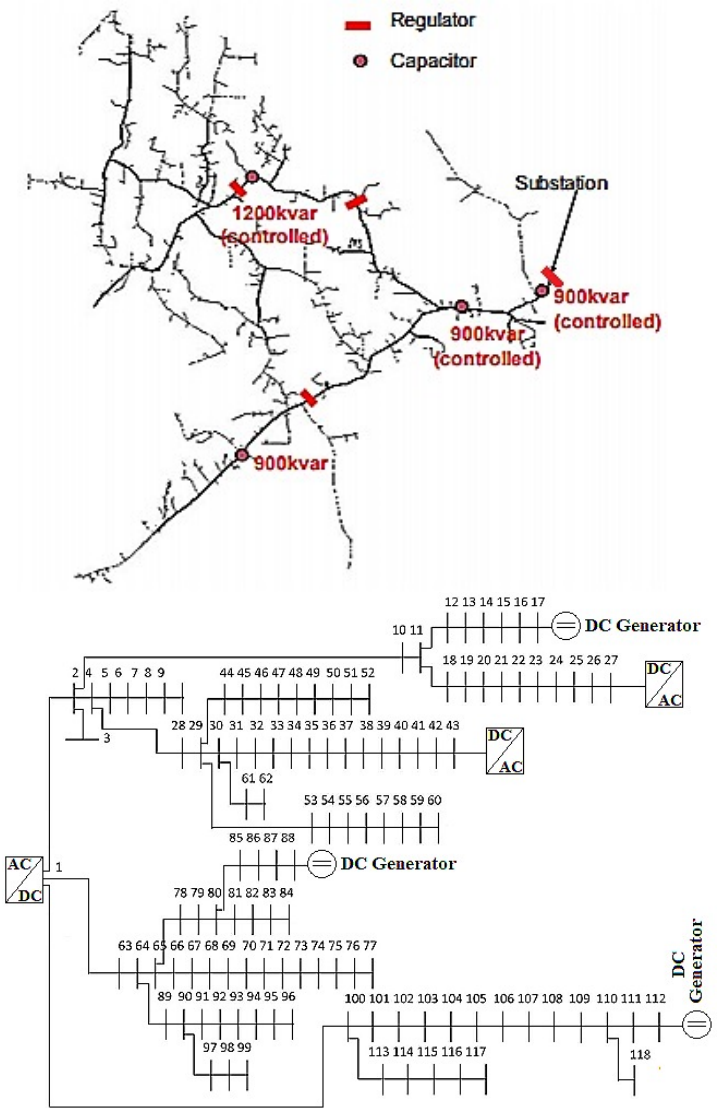

Fig. 1. From top to bottom: a) AC subgrid [1], b) DC subgrid

TABLE I
Parameters of DGs and IC

AC DGs: $K^{ac}_{P(i)}$ (i=70, 249, 458, 1500)	$1 \cdot 10^{-7}$ (Hz/W)
AC DGs: $K^{ac}_{Q(i)}$ (i=70, 249, 458, 1500)	$2 \cdot 10^{-4}$ (V/VAR)
AC DGs: $V^{ac}_{ref(i)}$ (i=70, 249, 458, 1500)	7.2 kV
AC DGs: $f_{ref(i)}$ (i=70, 249, 458, 1500)	50 Hz
AC DGs: P_{max}, S_{max}	4 MW, 5 MVA
SG-DG: Y_0	2.5 – 2.5·j
SG-DG: Y_2	2.5 – 2.5·j
DC DGs: $V^{dc}_{ref(i)}$ (i=17, 88, 112)	380 (V)
DC DGs: $K^{dc}_{P(i)}$ (i=17, 88, 112)	$2.5 \cdot 10^{-4}$ (V/W)

DC DGs: P_{max}	100 kW
ICs: f_{min}, f_{max}	49.5 Hz – 50.5 Hz
ICs: $V^{dc}_{IC,min}$, $V^{dc}_{IC,max}$	280V, 480V
ICs: Reactive power	0 kVar
ICs: Droop Gain $K^{IC}_{P(i)}$ (i=1, 27, 43)	$4 \cdot 10^{-6}$ (W^{-1})
ICs: S_{max}	60 kVA

B) Numerical Results of the AC subgrid

Figures 2a and 2b depict the phase-to-neutral voltages of the AC subgrid for two different regulations of SVRs:

➢ In Fig. 2a, all the SVRs are inactive (e.g their tap position is at the neutral point).

➢ In Fig. 2b, the SVRs between the buses 1057-1058 and 1311-1312 step up the phase-to-neutral voltage of each phase by 10%, while the other two SVRs remain inactive.

In all cases the capacitor banks are disconnected. To get a sense of the position of each bus in the network, their distance from the substation is depicted in Fig. 2c.

As shown in the voltage profiles, the network is highly unbalanced despite the connection of two DGs with voltage balancing capabilities. Thus the ability of the proposed approach, to solve the power flow in highly unbalanced large networks, is confirmed. Moreover, the proposed approach can effectively simulate the operation of SVRs.

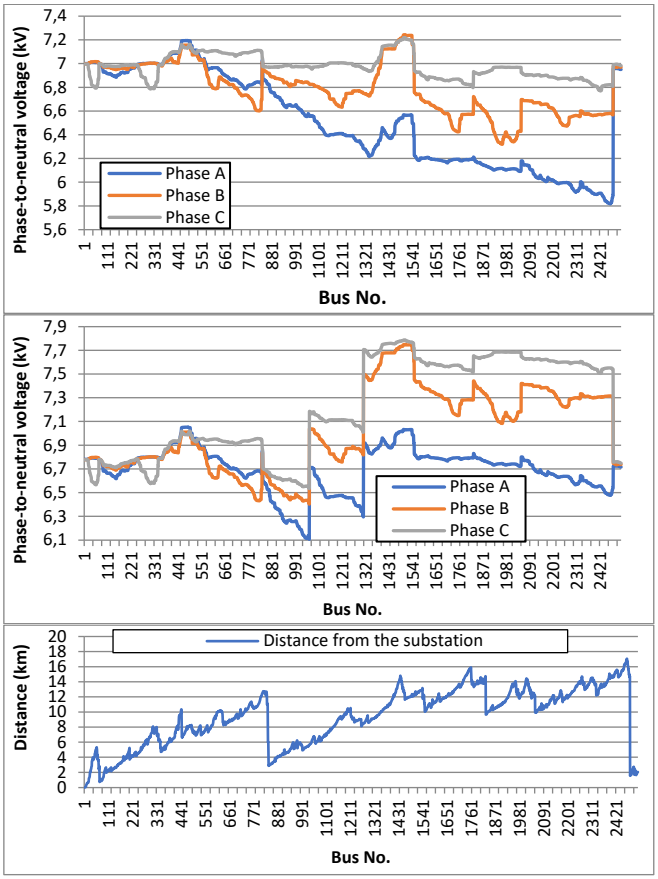

Fig. 2. From top to bottom: a) Voltage profile of the AC subgrid when SVRs are inactive. b) Voltage profile when 2 SVRs are activated, c) Distance of the AC buses from the substation.

Fig. 3 illustrates the neutral-to-ground voltage profile of the AC network for different grounding resistances. High grounding resistances result in a large ground potential rise (GPR) in some buses. It is common in some countries e.g North America, the MV distribution network to share the same grounding resistances with the LV secondary networks [3, Fig. 1]. As a result, the GPR of the MV network is transferred to the LV networks. Thus, due to the connection of the metal parts of an LV installation to the neutral conductor, a high GPR on the MV network can be sensed by the LV customers.

In recent years, complaints of GPR problems involving humans have become more frequent [3]. Utility companies and some of their customer groups have become increasingly interested in tools that can help troubleshoots GPR problems [3]. The proposed approach is the only power flow algorithm so far that can accurately estimate the GPR in hybrid AC/DC networks considering the realistic configuration of the network and DGs.

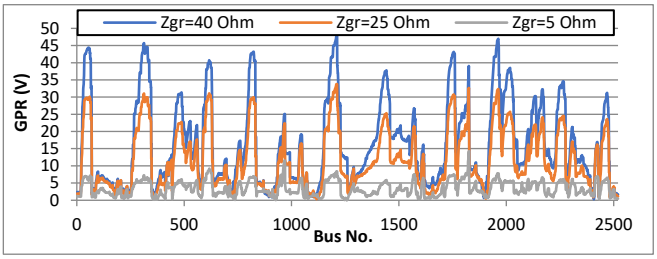

Fig. 3. Ground potential rise for various grounding resistances, when SVRs are inactive.

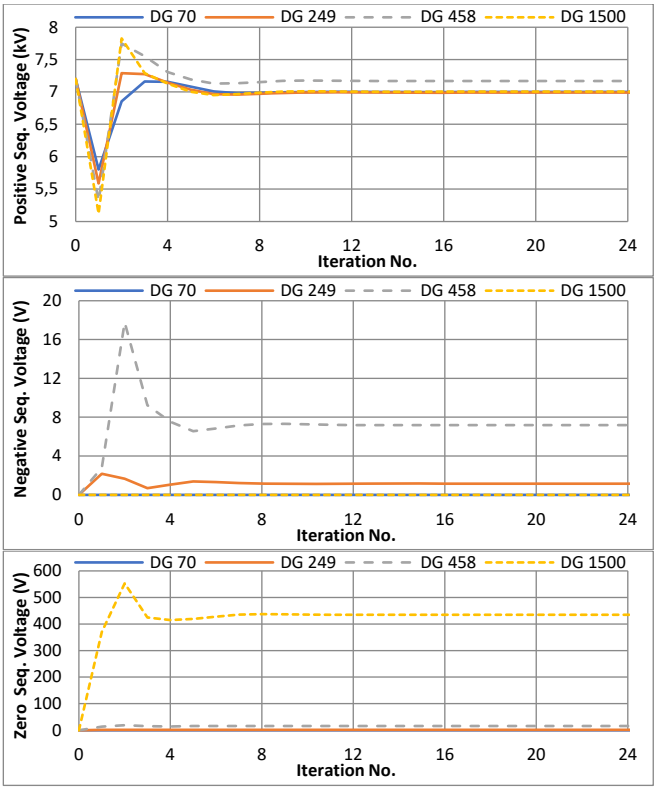

Fig. 4. From top to bottom: a) Positive-, b) Negative-, c) Zero-sequence voltage components of DC DGs. The SVRs are inactive.

The sequence voltage components of the AC DGs are depicted in Fig. 4. It is observed that the zero- and negative-sequence voltage components of the DG 70 are constantly zero throughout the iterative process. It is because of the implicit incorporation of these sequence components into the admittance matrix (see eq. (19) of the manuscript), resulting in an enhanced robustness and faster convergence compared with the explicit representation of [4]. Another interesting thing to note is the DG 1500, which is a three-wire DG with balanced pole-to-pole voltage, generating a

significant zero-sequence voltage component, while completely suppressing the negative-sequence voltage.

C) *Numerical Results of the DC subgrid*

Figures 5 and 6 depict the pole-to-neutral voltage profile and the GPR profile of the DC network, respectively. As shown, the voltage unbalance and the GPR at the buses near the DGs and ICs is negligible, due the voltage balancing and solid grounding of the DGs and ICs.

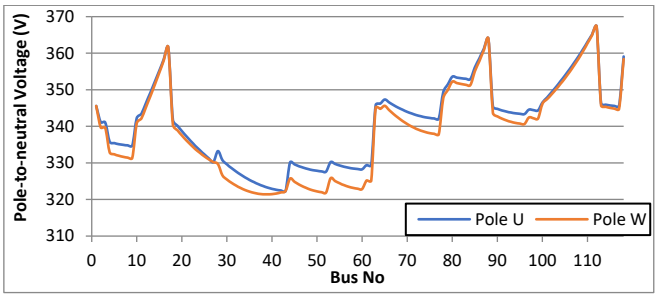

Fig. 5 Voltage profile of the DC subgrid

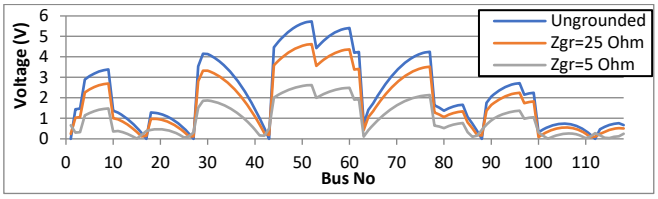

Fig. 6. Ground potential rise of the DC subgrid for various grounding resistances.

The differential- and common-mode voltage components of the DC DGs are depicted in Fig. 7. It is shown that the common-mode voltage component of all DGs is constantly zero throughout the iterative process due to the implicit expression of the common-mode admittances into the Y_{BUS} matrix (see eq. (35) of the manuscript).

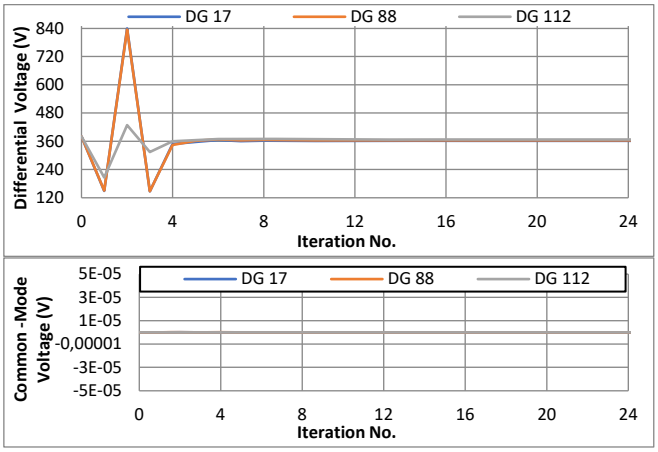

Fig. 7. From top to bottom: a) Differential-, b) Common-mode voltage components of DGs for the DC subgrid.

D) *Numerical Results of the ICs*

Fig. 8 shows the active power of the three ICs (P_{ic}), where a negative value denotes power transmission from the DC to AC subgrid. It is clarified that during the iterative process, a limiter at ±60kW was set to the power of IC, in order to prevent it from converging to a value higher than the maximum IC power. As shown, the powers of the three ICs converge to $(P_{ic1}, P_{ic27}, P_{ic43}) = (-54kW, -15.5kW, 4.18\,kW)$. In contrast to IC 1 and IC 27, the power of IC 43 is transmitted from the AC to DC subgrid due to the low voltage of DC bus 43.

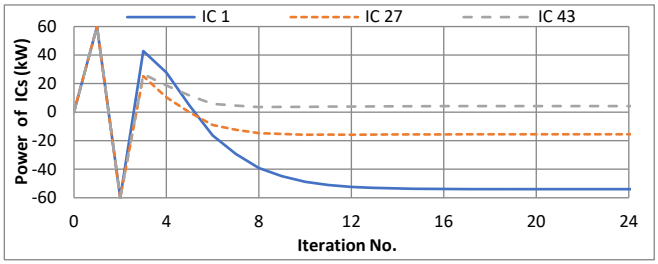

Fig. 8. Power of the ICs during the iterative process.

E) *Numerical Results of the Virtual Slack Nodes*

The active and reactive power of the virtual slack sources $(V^{ac}_{(0,a)}, V^{ac}_{(0,b)}, V^{ac}_{(0,c)}, V^{ac}_{(0,n)}, V^{ac}_{(0,g)})$ of Fig. 1 of the manuscript are depicted in Fig. 9a. The active power of the virtual slack sources $(V^{dc}_{(0,u)}, V^{dc}_{(0,w)}, V^{dc}_{(0,n)}, V^{dc}_{(0,g)})$ of Fig. 2 of the manuscript are depicted in Fig. 9b. As shown, the powers of all the virtual slack sources converge to zero after a small number of iterations, thus confirming that the subgrids operate as if they do not have slack buses.

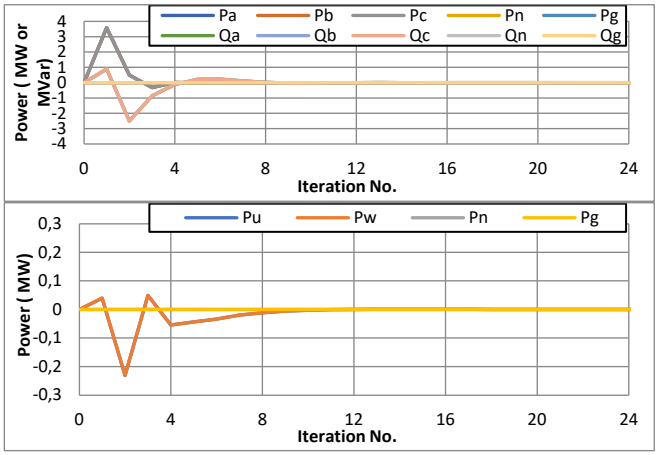

Fig. 9. From top to bottom: a) Active and reactive power of the sources of the AC virtual slack bus, b) Active power of the sources of the DC virtual slack bus.

F) *Execution Time of the Algorithm*

Finally, the execution time per iteration of the proposed algorithm is quoted in Fig. 10. The average execution time of the iteration is 0.26 sec. Since the algorithm needs 24 iterations to converge with an accuracy of 10^{-6} pu, the total execution time of the algorithm is 6.24 seconds.

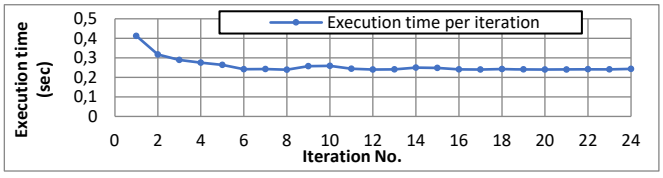

Fig. 10. Execution time of the algorithm per iteration

APPENDIX

All the AC buses that have been referred in this report correspond to the buses with the following reference names [2]: 70→M1209797, 249→226-23751, 458→M1069202, 750→M1026377, 800→M1026309, 817→L2804247, 1057→regxfmr_190-8581, 1058→190-8581, 1311→regxfmr_190-8593, 1312→190-8593, 1500→L3216351.

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[4] E.E Pompodakis, G.C Kryonidis, M. C Alexiadis, “A comprehensive load flow approach for grid-connected and islanded AC microgrids”, Trans. Power Systems, vol. 35, no. 2, pp. 1143-1155, 2020.