Ramp-Rate Limitation of Renewable Energy Sources for Voltage Quality Improvement in Distribution Networks: An Experimental Study

Stelios C. Dimoulias[a], Kyriaki-Nefeli D. Malamaki[a], Andrei Mihai Gross[b], Francisco de Paula García-López[b], Georgios C. Kryonidis[a], and Manuel Barragán-Villarejo[b]

[a] *Dept. of Electrical and Computer Engineering*, *Aristotle University of Thessaloniki*, Thessaloniki, Greece

[b] *Dept. of Electrical Engineering*, *Universidad de Sevilla*, Seville, Spain

steliosd@ece.auth.gr, kyriaki_nefeli@hotmail.com, amihai@us.es, fdpgarcia@us.es, kryonidi@ece.auth.gr, manuelbarragan@us.es

***Abstract*—The continuously increasing penetration of Converter-Interfaced Renewable Energy Sources (CI-RES) has posed various challenges to the electric grids, e.g., frequency instability, reverse power flows, power quality issues, etc. Regarding CI-RES connected to transmission systems, several regulations exist for limiting the CI-RES high active power ramp-rates (RRs), so as to reduce the conventional unit commitment and its associated, with the frequency-related Ancillary Services, costs. In Distribution Networks (DNs), no such specifications exist, even though high RRs, caused by the distributed CI-RES (CI-DRES), have been linked to rapid voltage changes (RVCs) and flickering phenomena, resulting in the reduction of voltage quality within DNs. In this paper, an RR limitation (RRL) method is incorporated in CI-DRES lab prototypes, equipped with Supercapacitors at their DC-link. These prototypes operate in a scaled-down version of the CIGRE Benchmark MV DN. The effect of the RRL on RVCs is studied with respect to two different RVC definitions, described in the IEEE 1547:2018 and IEC 61000-4-30:2015 Standards. The experiments reveal that the operation of CI-DRES, when incorporating a fast-acting energy storage system, can improve the voltage quality by mitigating the RVCs, considering both Standards' definitions.**

***Index Terms*—Ancillary Service, Active Distribution Networks, Energy Storage Systems, Ramp-Rate Limit, Rapid Voltage Changes, Voltage Quality**

I. Introduction

The stable and high-quality operation of electric grids is jeopardized by the ever-growing integration of Converter-Interfaced Renewable Energy Sources (CI-RES), as the latter are inertia-less, intermittent, and dispersed throughout power systems. Namely, issues like reverse power flows, power quality matters, frequency instability, etc. arise. To mitigate these issues, the Transmission System Operators (TSOs) have adopted various practices, such as conventional unit commitment, placement of central, large-scale Energy Storage Systems (ESS), [1], and ramp-rate limitation (RRL) via active power curtailment (APC), for CI-RES directly connected to the Transmission System (TS). Each solution has specific drawbacks, e.g., loss of income for the CI-RES owners, or the fact that only large energy market players are involved, [2], [3]. At Distribution Network (DN) level, the DN Operators are responsible for preserving the voltage quality within their DNs. Besides the reverse power flows and overvoltages reported, [2], the increased penetration of distributed CI-RES (CI-DRES) results in high Ramp-Rates (RRs), which, in turn, increase the number of rapid voltage changes (RVCs). RVCs affect the performance of equipment and produce flicker, inevitably compromising the DN voltage quality, [4], [5]. For this reason, voltage quality standards like EN50160 and IEEE 519, specify limits on the number of RVCs, within a specific time period. To tackle the RVCs in DNs, while also avoiding APC, a promising solution is the RRL of CI-DRES active power, [5]–[7], through ESS used with CI-DRES.

In this direction, various RRL methods have been proposed for different types of the CI-DRES primary source, i.e., sun [5], [6], and wind [8]; or different ESS types, e.g., Battery ESS (BESS), [7]–[10], Supercapacitors (SCs), [3], [11], or hybrid ESS, [12]. These methods can be categorized as [13]: a) moving average techniques, [14]; b) filter-based approaches, (low-pass filter, [5], Gaussian, [8], Kalman, [9], [12], Savitzky Golay, [10], etc.); c) direct RRL methods, [3]. Nevertheless, review and comparative studies, [11], [13]–[16], proved that direct RRL methods outperform others in terms of required ESS capacity and ESS charging/discharging cycles for given RRL level, [3]. In addition, it shall be mentioned that most studies consider an RRL=10 %/min, with respect to the CI-DRES primary source, without specifying the required RRL to reduce RVCs and flicker. However, this RRL value is too strict and should be re-assessed, [1]. Note that in this paper, RRL stands for the general practice of limiting the rate of change of active power (RoCoP), while the target limit of RoCoP, imposed by a certain RRL method, is denoted as RRL.

Regarding the impact of RRL on voltage quality, the literature is limited. In [5], the RRL method is employed in PV systems with ESS to alleviate voltage fluctuations, focusing on the ESS techno-economic feasibility and using, as a performance index, the 1-minute flicker effect. The analysis is conducted by means of power flow simulations using 1-minute data. Nevertheless, this study does not concern RVCs, since, based on the definitions provided in both IEEE 1547:2018 Standard (Std), [17] and IEC 61000-4-30:2015-

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Class A Std, [18], 1-second (1-s) average voltages should be considered for the RVCs examination. Moreover, the use of the flicker effect as a metric of voltage fluctuations is deemed as outdated, since it is based upon incadescent lamps and does not consider the broader impact of voltage fluctuations on the performance of equipment. In [6], [7], simulations in an LV DN demonstrated that the use of BESS for RRL can contain the fast variations of voltage/power, caused by the wind or sun, within the acceptable limits, as specified in the IEEE 1547:2018 Std, [17]. However, the use of BESS should be avoided for RVCs since the involved dynamics are much slower, [1], [11] and faster ESS, e.g., SCs, should be preferred for RRL in DNs, [3], [11], [15]. Furthermore, in [6], [7], the guidelines of [18] are not considered. In addition, regarding the Stds, several critical aspects of their definitions remain unclear. For instance, in [4], the authors highlight the: a) lack of a method for the estimation of the rate of change of voltage (RoCoV, dv/dt) during the event; b) the absence of specification for a minimum RoCoV to classify a voltage fluctuation as an RVC, as observed in the IEC 61000-4-30:2015-Class A. None of the considered studies addresses these issues.

Towards this direction, in this paper, the impact of RRL on RVCs within MV DNs is evaluated, according to two different Stds. Namely, the RRL method of [3] is incorporated in three CI-DRES lab prototypes (developed in the frame of the H2020 project EASY-RES [19]), within the scaled-down CIGRE MV DN, presented in [20], [21]. Each CI-DRES has an SC coupled at its DC link in order to limit the CI-DRES RRs. The results consider two different definitions of RVCs provided in [17], [18]. More specifically, half-cycle ($10ms$/50Hz) RMS measurements will be provided at substation level according to the Class A definition of [18]; while measurements of $0.5s$ will be provided at each node, considering different RRL levels and the RVC definition given in [17]. Both types of results will be used to evaluate the RRL impact on the RVCs. It is noted that such a comparative study, employing real measurements and fast-acting ESS, from the RVC-suppression point of view, was missing from the literature. This investigation: a) raises awareness about the relatively new voltage quality index of RVCs, highlighting the deficiencies and ambiguities in the definitions of the relevant Stds; b) paves a path so that the RRL employment, for the RVC-suppression, can be treated as a new, voltage-related ancillary service (AS). This AS could be provided not only within DNs, but also to the upstream TS, being in line with the requirements of the IEEE 2800-2022 Std, about CI-RES connected to TS.

The rest of the manuscript is organized as follows: Section II provides a brief revision of the IEEE and IEC definitions for RVCs, [17], [18]. Section III presents the RRL algorithm and the MV DN under study and describes the tests to be followed. Section IV presents and discusses the results. Finally, Section V closes the paper with its main findings, and proposes new directions for further research.

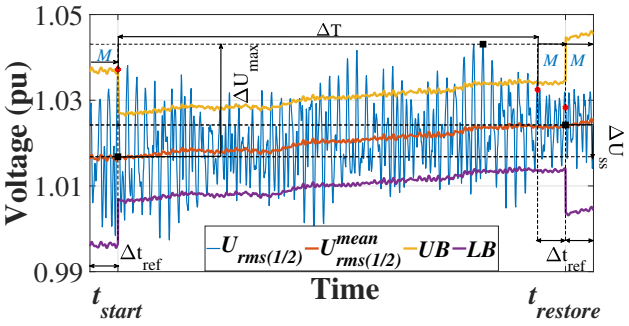

Fig. 1. Indicative RVC event according to [18]

II. RVCs: Revision of Standards

In this section, the IEEE 1547:2018 Std, [17] and IEC 61000-4-30:2015-Class A, [18] are briefly described, regarding the definition of RVCs. The perception of a specific RVC may vary depending on, [7]: a) the duration of a steady-state condition between two voltage changes; b) the RoCoV dv/dt; c) the magnitude of the voltage change. In this paper, the results are analyzed in the context of both Stds, to assess whether the CI-DRES fluctuations can cause excessive number of voltage variations per 1-s.

A. IEC 61000-4-30 Std

According to the IEC 61000-4-30:2015 Std.-Class A, [18], the RVC event detection is based on the $U_{\text{rms(1/2)}}$ magnitude, i.e the RMS value of the monitored voltage, U_{din}, measured over one cycle, and refreshed each half-cycle ($10ms$/50Hz). As stated in this Std, U_{din} is considered to be in steady-state, if all the M immediately preceding $U_{\text{rms(1/2)}}$ values lie within a dynamic threshold, calculated as a percentage of their arithmetic mean, $U^{\text{mean}}_{\text{rms(1/2)}}$, [4]. Therefore, an RVC event commences when at least one of the M immediately preceding values exceeds the dynamic threshold of $U^{\text{mean}}_{\text{rms(1/2)}}$. Respectively, the steady-state is restored when all the M immediately preceding $U_{\text{rms(1/2)}}$ values fall within the dynamic threshold. Henceforth, the commencing instant and the steady-state restoration instant of an event will be denoted as t_{start} and t_{restore}, respectively; while their difference, $\Delta t_{\text{unsteady}} = t_{\text{restore}} - t_{\text{start}}$, represents the time that U_{din} is not in steady-state. It shall be highlighted that, during the RVC event (i.e from its initiation until the steady-state restoration), a hysteresis is applied at the percentage of $U^{\text{mean}}_{\text{rms(1/2)}}$ that defines the threshold. The cardinality, M, of the examined values is defined as the number of values calculated within the reference time period $\Delta t_{\text{ref}} = 1\ s$, hence corresponding to $M = 100$ and $M = 120$, for 50 Hz and 60 Hz systems, respectively.

In [18], percentages from 1% to 6% of U_{din} for the detection threshold, $th(\%)$; and, in turn, around 50% of th, for the hysteresis, are suggested. Therefore, no strict directive exists and both parameters remain user-defined. This is further commented in Section IV.

Generally, an RVC is characterized in [18] by three parameters: duration (ΔT), magnitude (ΔU_{ss}), and maximum deviation (ΔU_{max}). ΔU_{ss} is defined as the absolute difference between the final $U^{\text{mean}}_{\text{rms(1/2)}}$value just prior to the event and

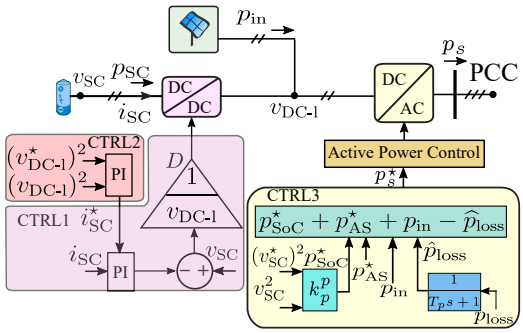

Fig. 2. Hierarchical CI-DRES control structure, [3], [22]

the first $U^{\text{mean}}_{\text{rms(1/2)}}$ value after the event. ΔU_{max} is defined as the maximum absolute difference between any of the $U_{\text{rms(1/2)}}$ values, during the RVC event, and the final $U^{\text{mean}}_{\text{rms(1/2)}}$value, just prior to the event. ΔT is defined as $\Delta T = \Delta t_{\text{unsteady}} - \Delta t_{\text{ref}} = t_{\text{restore}} - t_{\text{start}} - \Delta t_{\text{ref}}$. Provided that Δt_{ref} corresponds to the time needed for M $U_{\text{rms(1/2)}}$ values to be calculated, and that the restoration of the steady-state requires for M such values to lie within the threshold, ΔT implicitly expresses the elapsed time until the first $U_{\text{rms(1/2)}}$ falls within the threshold, with respect to t_{start}. Note that if the voltage variation is higher than ±10% of U_{din}, the voltage event is not considered as an RVC, but rather classified as a voltage swell or dip, respectively. For the better understanding of the detection process, the reader is referred to Fig. 1, where an indicative RVC event is identified, with all its characteristic parameters. In this case, $th = 2$ %, while UB, LB stand for the upper and lower boundary of the voltage, as calculated with respect to th and $U^{\text{mean}}_{\text{rms(1/2)}}$. Note the application of the hysteresis at the dynamic threshold, once an RVC occurs. The threshold is removed once the steady-state is restored.

B. IEEE 1547-2018 Std

The IEEE 1547:2018 Std defines that a CI-DRES shall not cause step or ramp changes in the RMS voltage at its Point of Common Coupling (PCC), exceeding 5% of nominal and exceeding 5% per 1-s, averaged over a period of 1-s, for the MV level; for the LV level this limit is 3%. As noticed, even though the thresholds are explicitly defined, no guidelines regarding the detection process are provided.

III. System Under Study

In this section, the RRL control applied to the CI-DRES, the CI-DRES topology and the MV DN under study are described.

A. RRL Control

The H2020 project EASY-RES [19] has proposed the use of SCs at CI-DRES level for RRL control to the CI-DRES power, [3]. In [3], a new direct RRL control method has been developed and compared to other state-of-the-art approaches. The CI-DRES is interfaced with the grid via a DC/AC Voltage Source Converter (VSC). The primary source is connected to the VSC DC-link, where there is also a connection with the SC, through a bidirectional DC/DC converter, as depicted in Fig. 2. In this configuration, the hierarchical, three-level control structure of [22] is adopted: SC current control loop

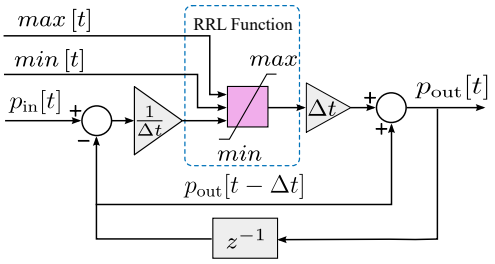

Fig. 3. Dynamic RRL, [3]

(CTRL1), DC-link voltage control loop (CTRL2) and SC voltage control loop (CTRL3). The first two control loops are used to control the VSC DC-link voltage through classic cascade control. CTRL3 generates the reference signal sent to the VSC, $p_s^\star$, which is computed based on the DRES active power, p_{in}, the power losses incurred in the VSC and the DC/DC converter, the State-of-Charge (SoC) power value, p_{SoC}, and the reference SC power, $p^\star_{\text{AS}}$, which is determined by the RRL control. CTRL3 aims to maintain the SC voltage, and this is reflected via p_{SoC}. The interface among the different control loops are analyzed in [22].

The RRL algorithm is depicted in Fig. 3 and Algorithm 1. The inputs are the DRES power, $p_{\text{in}}[t]$, the maximum ($max[t]$) and minimum ($min[t]$) limits of RRL. These limits are re-adjusted each Δt, depending on the SC SoC: based on the SC voltage, the RRL takes either a nominal value $\pm r_n$ (defined by the TSO or DNO considering both ramp-ups and ramp-downs) or follows a linear degradation - this is an alert area operation. In this way, the SC SoC is *a-priori* considered, re-adjusting the RRL, in order to ensure that even when the SC SoC is close to its limits, the RRL is still provided. The output of the control block is the smoothed power $p_{\text{out}}[t]$. After applying the algorithm, the reference power for the SC is $p^\star_{\text{AS}}[t]$. Details can be found [3].

Algorithm 1 Algorithm for RRL Function

Require: $p_{\text{in}}[t]$, $p_{\text{out}}[t - \Delta t]$, $min[t]$, $max[t]$, Δt
Ensure: $p_{\text{out}}[t]$, $p^\star_{\text{SC}}[t]$

$RR_{\text{succes-instant-calc}} \leftarrow \dfrac{p_{\text{in}}[t] - p_{\text{out}}[t - \Delta t]}{\Delta t}$
if $RR < min[t]$ **then**
  $RR \leftarrow min[t]$
else if $RR > max[t]$ **then**
  $RR \leftarrow max[t]$
else
  $RR \leftarrow RR_{\text{succes-instant-calc}}$
end if
$p_{\text{out}}[t] \leftarrow RR \cdot \Delta t + p_{\text{out}}[t - \Delta t]$
$p^\star_{\text{AS}}[t] \leftarrow p_{\text{in}}[t] - p_{\text{out}}[t]$

This control scheme is incorporated in three lab EASY-RES prototypes (ERPs). More specifically, the ERPs are 20-kVA three-phase, three-wire VSCs with V^{DC}_{rated}=750 V and V^{AC}_{rated}= 400 V. The coupled SCs are of 6 F rated capacitance and 160 V rated voltage with maximum instantaneous power of 2 kW. Note that the total SC energy is 21.33 Wh, however, due to the limitations of the DC/DC converter control the

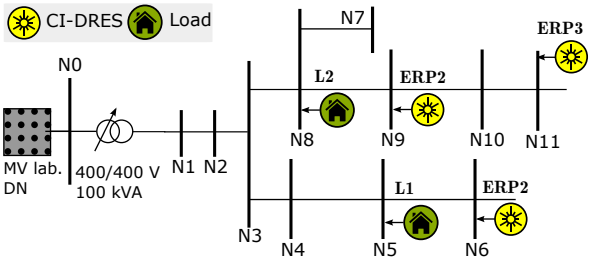

Fig. 4. Single-line diagram of the MV DN used for validation purposes, [20].

minimum voltage of the SC is 90 V. Hence, the total SC energy used for RRL control is equal to 9.33 Wh. A controllable current source emulates the primary energy source. The proposed control algorithm has been implemented in a Texas Instruments TMS320F28335 Delfino microcontroller with a sampling frequency of 20 kHz, thus 50 μs sampling rate. More details can be found in [3], [22].

In this paper, the study case regards the ejection of an artificial, step-profiled active power to emulate the active power of the ERPs primary source (p_{in}), for a 300-s analysis period, in order to demonstrate the performance of the RRL control and show the effect of the most severe RRs within the provision of the RRL functionality. Three different RRL scenarios (no RRL algorithm employed, RRL=200 W/s, and RRL=100 W/s) are concerned. Provided that the rated power of the ERPs is 20 kVA, the employed RRL values are lax, compared to the commonly suggested limit of 10 %/min (this would correspond to a target limit of 33.33 W/s in this case). However, these values are too strict for the specific SC size. Imposing an RRL of 10-50 W/s would destroy the SC.

B. Scaled-down CIGRE Benchmark MV DN

The system under study is the scaled-down CIGRE Benchmark MV DN presented in [20], [21], set in the lab of Universidad de Sevilla. This DN has been widely used in the technical literature due to the advantages it provides, including accessibility to conductor and profile parameters, CI-DRES, and flexible link integration. The original DN topology consists of two radial feeders, with a length of 15 km and 8 km, respectively. It is noted that for these experiments, only subsystem 1 of the scaled-down MV DN [21] has been used and the respective single-line diagram is depicted in Fig. 4. This subsystem contains a total of 11 buses, including two loads and three ERPs. The scaled-down DN has been designed by applying a change in the base magnitudes of the original grid, from 20 kV and 10 MVA, to 400 V and 100 kVA, respectively; allowing to reproduce the performance in a per unit basis of voltage drops, power flows, and power losses, in an LV laboratory. Fig. 5 (a) shows the two DN feeders, the branches that constitute it, and the cabinets that contains the devices used to emulate loads and/or CI-DRES. Fig. 5 (b) shows the inside of a cabinet,where the different components that constitute the devices emulating loads or CI-DRES are situated. Details of the topology and parameters of the MV DN, as well as the control and communication architecture for controlling the testbed in real time are given in [20], [21].

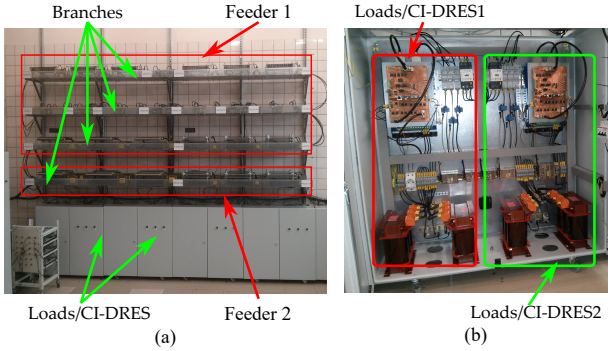

Fig. 5. Lab Scaled-down MV DN; (a) DN overview, (b) Cabinet interior

IV. Results

As stated in Section II, the RVC suppressing capability of the implemented RRL control, is assessed according to two different Stds, IEEE 1547:2018 and IEC 61000-4-30:2015-Class A. The two Stds differ regarding the required sampling rate of the monitored voltage U_{din} and the type of measurements. Namely, provided that the IEC Std. is based on the $U_{\text{rms(1/2)}}$ concept, instantaneous measurements, with a sampling rate of at least 10 ms, are required. Conversely, the type of measurements and the required sampling rate are undefined in IEEE 1547:2018. The only specification concerns the examination of RoCoV over a period of 1-s, without further details. Therefore, any sampling period of at least 0.5 s could be used. Due to the different resolutions of the voltage-measuring devices connected at each node, [3]: (a) RMS measurements, with a resolution of 0.5 s, were available for Nodes 2-11; (b) Instantaneous measurements, sampled every 50 μs, were available for Node 1. Consequently, the RVC-suppressing capability was evaluated with respect to IEEE 1547:2018 for the voltages of Nodes 2-11; and with respect to IEC Std. for the voltage of Node 1. More specifically, as shown in Fig 4, the nodes of major interest are Nodes 5 and 8, where the loads are connected (L1 and L2, respectively); and Nodes 6, 9, and 11, where the ERPs are connected (ERP1, ERP2, and ERP3, respectively).

The effect of the proposed RRL algorithm on the ERP2 active power is indicated in Fig. 6. Similar power profiles are obtained for the remaining ERPs, as well. The achieved capability of the employed RRL algorithm to suppress RVC phenomena is depicted in Fig. 7, where for space concerns, only results for an indicative Load Node (i.e. Node 8) and an indicative ERP Node (i.e. Node 6) are depicted, with similar results and conclusions applying for the rest of the nodes, as well. Specifically, the left-column subfigures represent the original voltage profiles at Nodes 8 and 6; while the right-column subfigures depict the respective voltages, after the application of the RRL algorithm, with RRL=100 W/s.

After the RRL application, the detected RVC events are completely suppressed and the smoothness of the voltage profiles has been significantly improved. Note that the voltages of the ERP nodes present considerably more frequent and significant variations compared to the voltages of the load nodes due to being directly affected by the variations of the

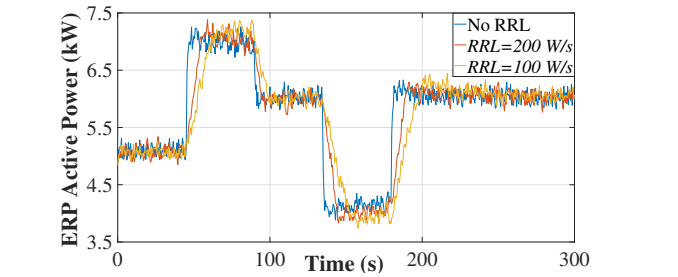

Fig. 6. Indicative ERP active power for different RRL levels

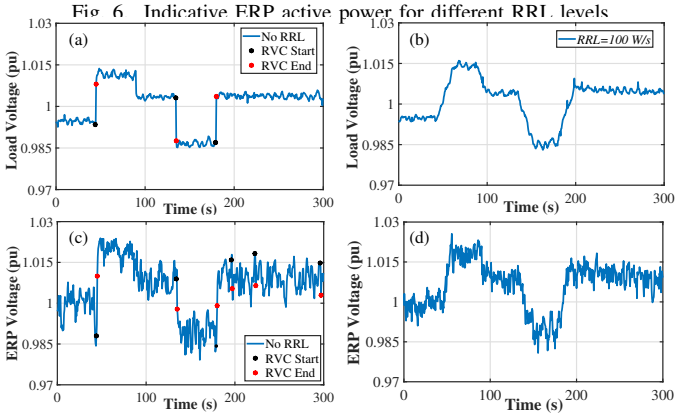

Fig. 7. Voltage profiles with respect to time: (a) Load Node Voltage - No RRL; (b) Load Node Voltage - RRL=100 W/s; (c) ERP Node Voltage - No RRL; (d) ERP Node Voltage -RRL=100 W/s

TABLE I
RVCs at ERP Nodes According to IEEE Std

	Node 6		Node 9		Node 11	
	N	$\frac{dV}{dt}$ $(\%/s)$	N	$\frac{dV}{dt}$ $(\%/s)$	N	$\frac{dV}{dt}$ $(\%/s)$
No RRL	6	1.99	5	1.44	5	1.44
RRL = 200 W/s	4	1.19	2	1.28	4	1.12
RRL = 100 W/s	0	-	0	-	0	-

primary energy source p_{in}. The overall effect of the RRL control is aggregated for all nodes and RRL levels in Tables I and II. The impact is quantified through the total number of RVC events, N, and the maximum RoCoV ($\frac{dV}{dt}$ (%/s)) measured for these N events. As shown, the application of an RRL of merely 200 W/s eliminates all the RVC events at Load Nodes. Regarding ERP Nodes, the same minimum level of RRL achieves an almost 40% reduction in the total number of events and their maximum RoCoV. Eventually, imposing an RRL=100 W/s completely eradicates the RVCs, ensuring the voltage quality in the DN. Moreover, note that the aptness of the conducted experiment is justified by the large number of triggered RVC events, i.e. at least N=3, for a period of 300 s (8.3% of an hour). Indeed, in the laxest scenario, the IEEE Std. limits the allowable number of RVCs to $2 \leq N \leq 10$ per hour.

The RVC-suppressing capability of the RRL control is further tested under the IEC definition, examining the changes in the voltage of Node 1. Prior to discussing the performance of the RRL control, it is important to comment on the strong dependency of the detection process and the characteristic magnitudes of the RVC events, on the user-defined detection threshold, $th(\%)$. This dependency is observed in Fig. 8,

TABLE II
RVCs at Load Nodes According to IEEE Std

	Node 5		Node 8	
	N	$\frac{dV}{dt}$ $(\%/s)$	N	$\frac{dV}{dt}$ $(\%/s)$
No RRL	3	1.78	3	1.66
RRL =200 W/s	0	-	0	-
RRL =100 W/s	0	-	0	-

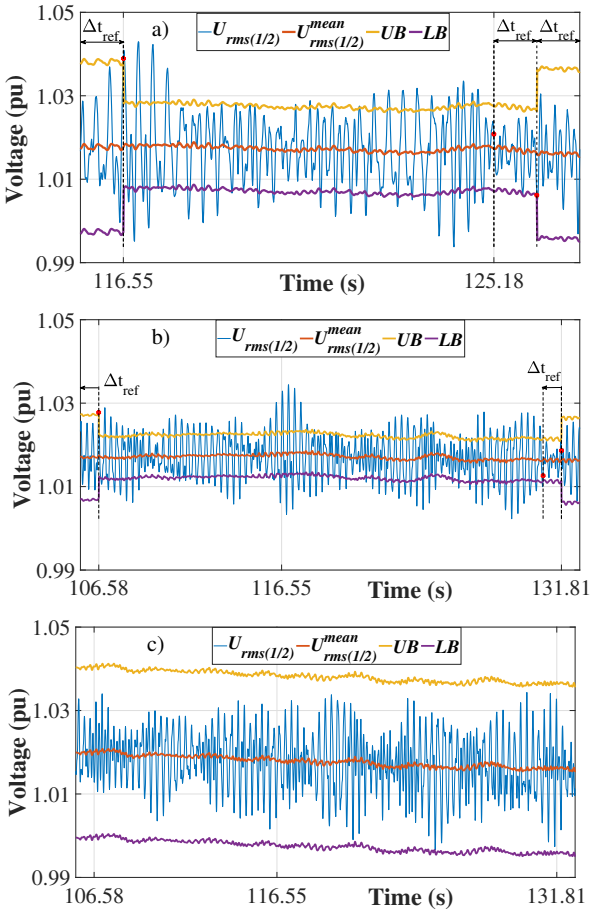

Fig. 8. RVC event detection: (a) $th = 2\%$ - No RRL; (b) $th = 1\%$ - No RRL; (c) $th = 2\%$ - RRL=100 W/s

where a certain RVC event is depicted. Specifically, Fig. 8 (a), Fig. 8 (b) represent the same detected event, but for th=2% and th=1%, respectively. In the latter case, due to the stricter threshold, the ΔT and $\Delta t_{\text{unsteady}}$ parameters are higher, rendering the detection process more sensitive and the recovery of steady-state voltage longer in duration. For the sake of better comparison, the start time t_{start}=116.55 s of the event, under the th=2% consideration, is also stamped at Fig. 8 (b). As observed in Fig. 8 (c), the implementation of the proposed algorithm with RRL=100 W/s suppresses the event, containing the voltage between the required upper (UB) and lower boundary (LB).

The overall results for the 300-s analysis period are aggregated in Table III, with respect to the total number of events and the implied maximum values of the characteristic parameters, for the N events. As shown, the implemented algorithm effectively mitigates the RVCs, reducing their number,

TABLE III
RVCs ACCORDING TO IEC

	$th = 2\%$			
	N	ΔU_{max} (%)	ΔU_{ss} (%)	ΔT (s)
No RRL	13	2.63	0.74	28.17
RRL=200 W/s	3	2.83	0.12	1.58
RRL=100 W/s	1	2.08	0.10	0.31
	$th = 1\%$			
No RRL	24	2.67	0.70	39.19
RRL=200 W/s	6	2.94	0.28	8.81
RRL=100 W/s	2	1.92	0.13	1.37

duration, and long-term magnitude. Regarding the number of detected N events for different RRL and th values, it is shown that N is almost doubled by reducing th at 1%. For both values of th, when applying different RRL, the number of events N is reduced by 75-92%. The appropriate values of th and RRL should be further investigated in terms of ESS sizing, cost and cycling, because strict limits might result in unnecessary ESS fatigue. Regarding the stochastic parameter of ΔU_{max}, it is observed that in the case of RRL=200 W/s, higher maximum values are presented, compared to the original case. This finding could indicate the general inability of such a loose RRL to drastically contain the voltage, in the time scale of milliseconds. This anomaly and the further investigation of the method according to the IEC Std is a subject for further research.

V. DISCUSSION AND CONCLUSIONS

In this paper, the performance of a direct RRL algorithm, implemented in three CI-DRES lab prototypes was evaluated, in terms of its RVC-suppression capability. The evaluation concerned real measurements from a scaled-down version of the CIGRE MV benchmark distribution network and was based on the guidelines of the respective IEEE and IEC Stds. The findings demonstrated that the proposed RRL control could improve the voltage quality within the distribution network, significantly mitigating the RVCs that might occur due to rapid variations of CI-DRES active power. In addition, the proposed algorithm improved the voltage quality at the Point of Interconnection of the distribution network with the upstream transmission system. This means that the coordinated and decentralized RRL from the CI-DRES within a distribution network could offer a new voltage-related service to the upstream transmission system. Therefore, the conducted analysis could pave way for the recognition of the RVC elimination as a new service, to be remunerated in respective markets. Towards this direction, further research will be conducted for the mathematization of the RVC alleviation capability with respect to a distribution network's natural parameters (i.e. line length, impedances and general topology), in order to untap the potential of coordinated control of the individual sources.

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