Energy Management In Converter-Interfaced Renewable Energy Sources Through Ultracapacitors For Provision Of Ancillary Services

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***Abstract*—The ever-growing penetration of Converter-Interfaced Distributed Renewable Energy Sources (CI-DRES) and the gradual decommission of synchronous generators (SGs) has posed several challenges related to the stability and robustness of the electric power systems. Since the main interface of the CI-DRES with the grid are the Voltage Source Converters (VSCs), there has been a major shift in the VSC control philosophy, where the absence of SGs is compensated by the Ancillary Services (ASs) provided by a new generation of CI-DRES. In order to make these ASs feasible and emulate the dynamic behaviour of a SG, the presence and advanced control of energy storage systems (ESS) together with the CI-DRES is essential, so that the CI-DRES/ESS has a dynamic behaviour similar to SG. In this paper, a new energy management control system is proposed for an ultracapacitor (UC) connected to the DC-bus of a CI-DRES. The aim is to control the DC bus voltage using the UC and, simultaneously, maintain the UC voltage within the limits while a given AS is provided. The control strategy is validated experimentally using a prototype with results revealing a reliable and stable operation.**

***Index Terms*—renewable generation, ancillary services, energy storage systems, ultracapacitors, voltage source converters, supercapacitors, renewable energy source**

I. Introduction

During the past two decades, the new advances in Renewable Energy Sources (RES) have initiated a major shift towards a decentralized, decarbonized non-synchronous generation. This shift is further encouraged by the European Union with proposals concerning the 2030 Climate & Energy Package, aiming to achieve an increase of 32% of RES penetration and a reduction of 40% in greenhouse gas emissions (with respect to 1990) until 2030 [1]. The main interface of the RES with the grid are the Voltage-Source Converters (VSCs). As the level of the Converter-Interfaced Distributed RES (CI-DRES) increases displacing conventional generation units, several serious problems are revealed related to the dynamic performance and stability of the power systems. These problems stem from the intermittent nature of the primary energy source (wind, sun), the nature of the VSCs - i.e. the fact that they do not possess any inherent inertia and the VSC current operation mode, i.e. delivery of the maximum possible power from the primary source.

On the bright side, the VSCs have an important control capability for solving these problems. Recently, several control algorithms have been proposed in the technical literature with the objective that the VSC emulates the behavior of a synchronous generator (SG). In this way, a series of ancillary services (ASs) can be provided to the network such as: primary frequency regulation (PFR) -i.e. operation with *P-f* droop-, [2], [3], ramp-rate limitation (RRL) - also referred as power smoothing (PS) - [4], [5], Fault-ride through (FRT) [6], and virtual inertia (VI) [7]–[10], that will help the operation and stability of the future electrical network dominated by RES. However, the provision of ASs that require active power management (RRL, VI, FRT) will imply that the DRES has to work away from its maximum power point tracking (MPPT). This will cause economic losses to the DRES owner if these ASs are not properly remunerated. As an alternative, for this type of ASs, the CI-DRES VSC is usually equipped with an Energy Storage System (ESS) keeping its operation in MPPT. For ASs that require fast response by the ESS (e.g. VI or high-frequency PS) a short-term ESS like an Ultracapacitor (UC) is more appropriate. For ASs with slower time evolution and higher energy amounts (e.g. PFR or Low-Frequency PS) an electrochemical ESS, like a Battery (BESS), is more suitable.

An efficient way to integrate the ESS into a PV inverter is to connect it to the VSC DC bus through a DC/DC converter, since the voltage levels of both devices are different as shown in Fig. 1. In this manner, the control capacity of the system is also increased compared to the traditional control of a CI-DRES VSC. This traditional operation is based on the control of the injected current of the ESS through the DC/DC converter on the one hand, and, on the other hand, on the control of the DC bus voltage through the VSC [11], enabling, the power delivery of both the PV plant and the ESS at the VSC Point of Interconnection (POI). However, the traditional operation of the CIDRES-VSC/ESS limits the VSC capability to emulate a SG and provide the ASs, due to the fact that in the latter case, it is essential to control the power injected at

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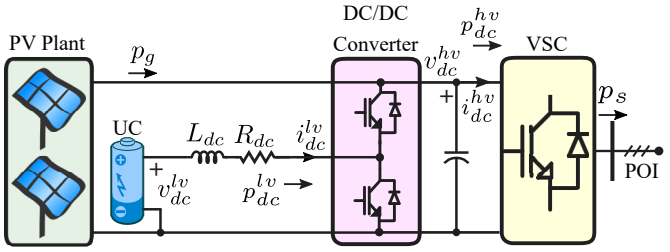

Fig. 1. CI-DRES comprising an ESS interfaced with a DC/DC converter.

the POI, p_s, [12] and not the DC bus voltage.

One possible solution would be to employ the ESS to control the DC bus voltage instead of VSC [13]. Thus, the VSC would have total controllability of the active power injected into its POI to provide ASs. Nevertheless, this proposal has certain limitations, since the maximum available active power p_s depends on ESS state of charge (SoC) and the power of the primary energy source, p_g. In order to guarantee a stable and reliable system operation before, during and after the ASs provision, a proper management of the ESS SoC becomes crucial, keeping it within the safe operating zone recommended by the ESS manufacturer, since the ESS is responsible to control the DC bus voltage.

With respect to the Energy Management System (EMS) of an ESS and its SoC for the provision of AS, the research main focus has been on BESS and particularly, the recovery after the BESS participation in the PFR [14], especially in islanded microgrids [15]. Regarding BESS and the provision of other ASs, in [16] different RRL control schemes and SoC methods have been proposed, so that the BESS returns to 50% SoC. However, these studies focus mainly on the provision of RRL not on the proper restoration of the BESS SoC. In case of fast-acting ESS, like the UC, little attention has been paid on the UC SoC for the provision of ASs. In [17], a control scheme for the UC SoC control is proposed, so that it returns to a region of 45-55% SoC after performing RRL. An UC SoC proportional controller is proposed in [6], where the UC returns to 50% SoC after performing RRL or FRT. Therefore, to the authors' best knowledge, there is a gap in the State-of-the-art that consists in providing a quality AS while the UC SoC is maintained properly.

The main contribution of this paper is to propose an efficient EMS of a CI-DRES comprising an UC so that at the same time the DRES can work in MPPT, provide high quality ASs and the UC SoC is within the technical limits allowed by the manufacturer. After the provision of the AS, the UC must have the ability to return to its reference voltage in order to be able to provide the required AS again in the future. The rest of the paper is organised as follows. Section II presents the control structure of the EMS. Section III describes a prototype used for the experimental validation of the control strategy and discusses the EMS performance via obtained results. Finally, Section IV closes the paper with the main conclusions.

II. EMS CONTROL STRATEGY

The control strategy of the EMS, performed by the DC/DC converter, is based on the control of the DC bus voltage by

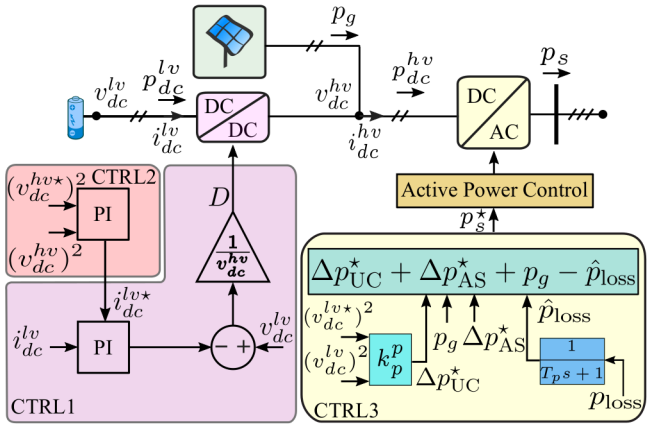

Fig. 2. ESS hierarchical control scheme for the DC-bus energy management.

regulating the current of the UC (ESS selected for this work). This means that any difference between the power from the primary energy source p_g and the VSC injected power p_s must be compensated by the UC. Therefore, the UC is responsible both for providing the requested active power during the AS provision and the DC bus voltage control. As a consequence, it is of utmost importance to maintain under control the UC SoC, so as to operate the system safely and reliably.

To achieve this goal, a hierarchical control structure composed of three levels is proposed in the EMS as depicted in Fig. 2: UC current control loop (CTRL1), DC bus voltage control loop (CTRL2) and UC voltage control loop (CTRL3). The first two control loops are used to control the VSC DC bus voltage through a classic cascade control. Meanwhile, the third control loop aims to maintain the UC voltage, and therefore, its SoC, within the technical limits recommended by the manufacturer and, simultaneously, must not interfere with the power required by the AS. Therefore, this control loop has to fulfill two objectives that in principle can be considered opposed: absorb or inject energy to keep the UC voltage within technical limits and release its energy during the provision of the AS. Each control loop and the interfaces among them are analyzed in the following subsections.

A. Current control loop (CTRL1)

This control loop corresponds to the inner control loop in the cascade control. Its aim is to generate the duty ratio of the DC/DC to properly control the current circulating through the inductive filter between the UC and the DC/DC converter. The input of this loop is the current reference computed in CTRL2 $i_{dc}^{lv\star}$ and its output is the DC/DC converter duty ratio D. The control law implemented is a proportional and integral (PI) controller which is designed from the average model of the DC/DC converter and the voltage drop between the UC and the converter itself:

$$v_{dc}^{lv} = i_{dc}^{lv} \cdot R_{dc} + L_{dc} \cdot \frac{di_{dc}^{lv}}{dt} + v_{dc}^{hv} \cdot D, \qquad (1)$$

where v_{dc}^{lv} and i_{dc}^{lv} are the UC voltage and current respectively, L_{dc} and R_{dc} are the inductance and the internal resistance of the DC filter respectively and v_{dc}^{hv} is the VSC DC bus voltage.

Applying a PI controller to this model, the duty ratio to operate the DC/DC converter is computed as:

$$D = \frac{v_{dc}^{lv} - k_p^i \left(i_{dc}^{lv\star} - i_{dc}^{lv}\right) - k_i^i \int \left(i_{dc}^{lv\star} - i_{dc}^{lv}\right) dt}{v_{dc}^{hv}}, \quad (2)$$

where k_p^i and k_i^i are the proportional and the integral gains of the PI controller respectively. These are designed by defining a desired closed-loop time constant τ_i as: $k_p^i = L_{dc}/\tau_i$ and $k_i^i = R_{dc}/\tau_i$.

B. DC bus voltage control loop (CTRL2)

This control loop corresponds to the outer control loop of the cascade controller and its aim is to control the voltage of the VSC DC bus. It is based on the power balance between the low and high voltage side of the DC/DC converter neglecting the power losses:

$$p_{dc}^{lv} = v_{dc}^{lv} \cdot i_{dc}^{lv} = p_{dc}^{hv} = v_{dc}^{hv} \cdot i_{dc}^{hv}, \quad (3)$$

where p_{dc}^{lv} is the power transferred from the low voltage side of the DC/DC converter, p_{dc}^{hv} is the power in the high voltage side of the DC/DC converter and i_{dc}^{hv} is the current in the high voltage side. This current can be related to the DC bus capacitor voltage C_{dc} as follows:

$$i_{dc}^{hv} = C_{dc} \cdot \frac{dv_{dc}^{hv}}{dt}, \quad (4)$$

and it can be replaced and operated in (3) as:

$$p_{dc}^{lv} = v_{dc}^{lv} \cdot i_{dc}^{lv} = v_{dc}^{hv} \cdot C_{dc} \cdot \frac{dv_{dc}^{hv}}{dt} = \frac{C_{dc}}{2} \frac{d(v_{dc}^{hv})^2}{dt}. \quad (5)$$

From this equation, which represents the plant of the system for the CTRL2, a PI controller can be applied to compute the required current reference $i_{dc}^{lv\star}$ in CTRL1:

$$i_{dc}^{lv\star} = \frac{k_p^v \left[(v_{dc}^{hv\star})^2 - (v_{dc}^{hv})^2\right] + k_i^v \int \left[v_{dc}^{hv\star})^2 - (v_{dc}^{hv})^2\right] dt}{v_{dc}^{lv}}, \quad (6)$$

where k_p^v and k_i^v are the proportional and the integral gains of the PI controller in CTRL2 respectively and $v_{dc}^{hv\star}$ is the desired voltage at the VSC DC bus. Note that the error is computed from the square of the voltages $v_{dc}^{hv\star}$ and v_{dc}^{hv}. The control gains k_p^v and k_i^v are designed by setting a closed-loop time constant τ_v of CTRL2 at least 10 times slower than CTRL1 as: $k_p^v = C_{dc}/\tau_v$ and $k_i^v = G_{sh}/\tau_v$. Term G_{sh} is the parallel conductance of the DC bus capacitor. This decision allows to neglect the inner dynamics of CTRL1 in CTRL2 [18]. In this way, both control loops can be independently designed without considering dynamics interaction between them.

C. UC voltage control loop (CTRL3)

This control level must satisfy two objectives simultaneously: i) maintain the UC voltage within the allowed technical limits (UC voltage is directly related to its SoC), and, ii) be flexible enough to release energy from the UC and provide the active power required for the provision of an AS.

The design of this control is based on the power balance of the total set-up in Fig. 1. According to this scheme, this power balance must fulfill:

$$p_{\text{UC}} = p_s - p_g + p_{\text{loss}}, \quad (7)$$

where p_{UC} is the UC active power and p_{loss} are the total power losses (including those of the DC/DC converter, DC filter, VSC and AC filter). If the primary active power p_g is injected into the grid by the VSC ($p_s = p_g$), the UC has to cope with the system power losses. However, if the power balance between p_s and p_g is not fulfilled due to the provision of an AS involving active power (like VI, RRL or PFR), it is required that the UC injects this difference $\Delta p_{\text{AS}} = p_s - p_g$ because this device is in charge of controlling the VSC DC bus. Therefore, the UC power must supply the following terms:

$$p_{\text{UC}} = \Delta p_{\text{AS}} + p_{\text{loss}}. \quad (8)$$

It is evident from these expressions that, regardless of whether the AS is provided or not, a continuous control of the UC SoC is required, since the power losses must be continuously supplied by the UC. If such control is not enabled, the UC would proceed to discharge enough to lead to the loss of the DC bus voltage control as well as the loss of control of the CI-DRES VSC. Hence, a proportional controller is proposed to absorb a given active power from the POI, $\Delta p_{\text{UC}}^\star$, and maintain the UC SoC:

$$\Delta p_{\text{UC}}^\star = k_p^p \cdot \left[(v_{dc}^{lv})^2 - (v_{dc}^{lv\star})^2\right]. \quad (9)$$

where $v_{dc}^{lv\star}$ is the desired UC voltage reference. The control law proposed in (9) is a proportional gain. This causes an error in steady-state that avoids reaching the desired value $v_{dc}^{lv\star}$. However, it allows the UC to release energy to provide AS, thus, fulfilling the two objectives of this control level. The design of the proportional gain is done in a similar way to CTRL2 simply by replacing the capacity value of the UC by the capacity of the VSC DC bus in (6). The value of this proportional gain is selected so that its closed-loop time constant is greater than the duration of the provision of the AS. In this way, the AS provision is affected as little as possible.

Taking this term into account, the desired power of the VSC injected at the POI $p_s^\star$ is defined as:

$$p_s^\star = \Delta p_{\text{AS}}^\star + p_g + \Delta p_{\text{UC}}^\star. \quad (10)$$

where $\Delta p_{\text{AS}}^\star$ is the term corresponding to the provided AS. The computation of this term goes beyond the scope of this paper, but more details can be found in [4], [5], [10], [19].

The power losses are not included in (10) and this implies that the UC must take care of them according to (8). Taking into account that these power losses can be significant, mainly due to the VSC and the DC/DC converter, the control law in (9) might not be enough to maintain the UC voltage within allowed limits. To mitigate this undesirable effect, it is proposed to add a new term in (10) corresponding to a feed-forward signal that compensates for the power losses. This strategy causes the power losses to be assumed by the VSC instead of the UC. This term cannot be directly added because it would affect the AS provision. Therefore, a low pass filter (LPF) is proposed to be applied to these losses to reduce its impact on the AS. The final reference of $p_s^\star$ remains as:

$$p_s^\star = \Delta p_{\text{UC}}^\star + \Delta p_{\text{AS}}^\star + p_g - \hat{p}_{\text{loss}}. \quad (11)$$

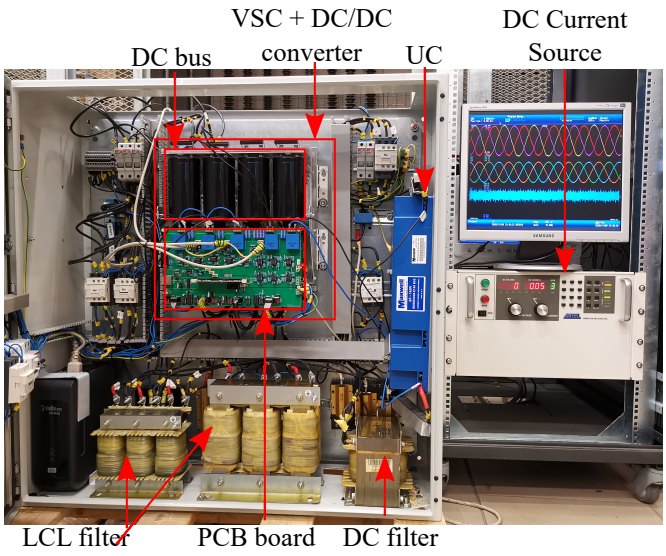

Fig. 3. Laboratory experimental testbed.

where $\hat{p}_{\text{loss}}$ is computed as:

$$\hat{p}_{\text{loss}} = p_{\text{loss}} \frac{1}{T_p s + 1} \; ; \; p_{\text{loss}} = p_{\text{UC}} + p_g - p_s. \qquad (12)$$

The time constant of the LPF T_p must be selected in a similar way to the proportional gain of (9), typically with a value similar to the duration time of the AS.

III. Experimental Testbed and Results

The hierarchical control structure of the EMS presented in the previous section is tested in the experimental setup depicted in Fig. 3. This has been developed at the Universidad de Sevilla under the framework of European project EASY-RES. The main components of the experimental testbed and controller gains are summarized in Table I. The proportional gain k_p^p and the LPF time constant T_p in CTRL3 will be detailed in the discussion of the experimental results. A brief description of the main components is made as follows: i) A three-phase three-wire VSC rated at 20 kVA with AC side coupled through a LCL filter to an AC controllable voltage source. The rated AC voltage and DC voltage are 400 V and 750 V respectively. This power converter is in charge of setting the power $p_s^\star$ and its control strategy is based on a virtual SG [7]. Therefore, it has the capacity of reacting under frequency events injecting/absorbing an extra power ($\Delta p_{\text{AS}}^\star$ term in (11)) corresponding to the VI; ii) An UC of 6 F and 160 V as ESS connected to the VSC DC bus through an inductive filter and a DC/DC converter; iii) A controllable DC current source connected to the DC bus of the VSC which is responsible of reproducing the active power injected by the RES.

The VSC and the DC/DC converter have been integrated in a common power electronic stack (four-leg VSC) to achieve a compact design. This enables the use of a single control board and microcontroller for both devices where the analogue measurements from the VSC, the DC/DC converter, the primary energy source, the corresponding IGBT switching signals and the proposed controller are centralized. In addition, this facilitates the possibility of exchanging data between the different control layers. The control algorithm has been implemented in a TMS320F28335 Delfino microcontroller provided by Texas Instruments with 20 kHz sampling frequency.

TABLE I
Parameters of the experimental setup and controller gains.

Parameter	Value
DC bus voltage (v_{dc}^{hv})	750 V
RMS AC VSC rated voltage	400 V
VSC rated power	20 kVA
VSC and DC/DC converter switching frequency	10 kHz
VSC side AC filter inductance	1.25 mH
Grid side AC filter inductance	1.25 mH
AC filter capacitance (C)	4 μF
DC/DC converter rated power	10 kW
DC/DC converter filter inductance (L_{dc})	3 mH
DC bus capacitor (C_{dc})	2200 μF
DC UC rated voltage	160 V
UC capacitance	6 F
Controllable DC source rated power	30 kW
τ_i. Closed-loop time constant of CTRL1	1.0 ms
k_p^i. Proportional gain of CTRL1	3.0
k_i^i. Integral gain of CTRL1	100.0
τ_v. Closed-loop time constant of CTRL2	1.0 ms
k_p^v. Proportional gain of CTRL2	0.0878
k_i^v. Integral gain of CTRL2	0.73185

Two types of tests are carried out in order to analyze how the proposed controller is affecting the AS provision and the UC voltage. The first set of tests consists of studying of influence of the proportional gain k_p^p in CTRL3. Three gains equal to 0.075, 0.15 and 0.3 are evaluated which correspond to a closed-loop time constant of 90 s, 40 s and 20 s respectively. The LPF time constant T_p selected for these tests is 30 s. The second group of tests studies the influence of this LPF time constant for the power losses compensation through three different values of T_p: 30 s, 15 s and 1 s, with a proportional gain k_p^p equal to 0.075. All tests are carried under the same experimental event. This consists on generating a negative frequency perturbation in the AC controllable voltage source during four seconds which causes a reaction of the virtual SG injecting an extra power $\Delta p_{\text{AS}}^\star$ to the POI equal to 2 kW.

Fig. 4 represents the active power p_s, p_g and p_{UC} for the first group of tests. In addition, the ideal response of powers p_s and p_{UC} under the frequency perturbation is illustrated in this figure. This corresponds to an ideal virtual SG without power losses and composed by an infinite voltage DC source instead of an UC. Note that the ideal power increase is 2 kW corresponding to the $\Delta p_{\text{AS}}^\star$ term. At the beginning of the test, the system is in steady-state and the powers for the different k_p^p values are identical. It can be observed that p_g is almost identical to p_s and p_{UC} is null because of the DC bus voltage and the UC voltage are under control as shown in Fig. 5. The power difference between p_g and p_s corresponds to the converter power losses. Around $t = 19s$, the frequency event is activated in the AC controllable source and the power p_s drastically increases from 6 kW to almost 8 kW. From this time instant, it can be observed that a lower value of k_p^p leads to delivery a power p_s and p_{UC} closer to the ideal response. As the frequency event advances in time, the power corresponding to the AS provision is progressively reduced with respect to the ideal response, reaching its lowest value at the end of the

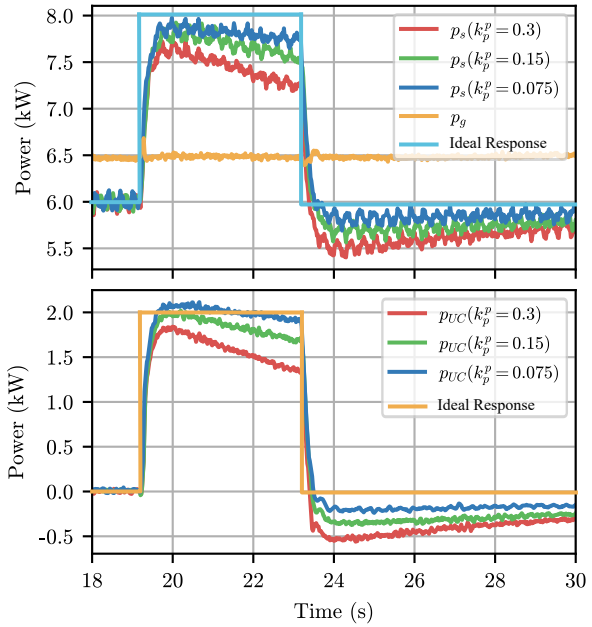

Fig. 4. Powers of the first group of tests. Top plot: Active power injected by the VSC at the POI for different k_p^p values and power from the primary energy source. Bottom plot: Active power injected by the UC for different k_p^p values.

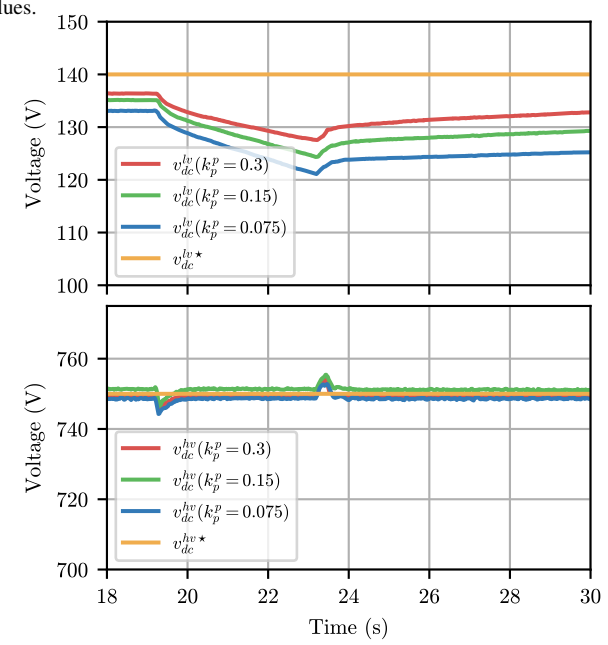

Fig. 5. Voltages of the first group of tests. Top plot: UC voltage evolution for different k_p^p values. Bottom plot: DC voltage bus evolution for different k_p^p values.

event around $t = 23s$. This reduction is greater with high values of k_p^p. Once the frequency event is over, both p_s and p_{UC} tend to return to their original values. Again, a lower value of k_p^p leads to a closer response to the ideal.

The previous behavior of p_s and p_{UC} occurs because the $\Delta p_{\text{UC}}^{\star}$ term for computing $p_s^{\star}$ in (11) directly depends on the value of k_p^p and the quadratic error of the UC voltage. A high value of k_p^p increases the value of this term, which reduces the AS provision reflected in both a lower power delivered by the UC p_{UC} and injected power to the POI p_s. This effect is also seen in the UC voltage evolution in the top plot of

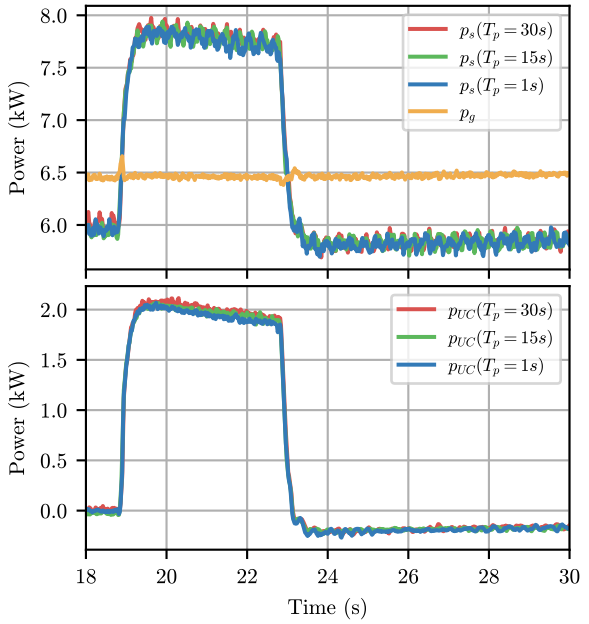

Fig. 6. Powers of the second group of tests. Top plot: Active power injected by the VSC at the POI for different LPF time constant T_p an power from the primary energy source. Bottom plot: Active power injected by the UC for different LPF time constant T_p.

Fig. 5. Increasing the gain k_p^p implies releasing less energy from the UC which is reflected in a lower voltage drop of the UC during the frequency event. In addition, high k_p^p values lead to a minor error in steady-state and faster UC voltage recovery after the frequency event is finished. The DC bus voltage evolution is depicted in the bottom plot of Fig. 5. An adequate and similar tracking is obtained for any k_p^p value except a little disturbance, which is quickly corrected, in the transitory periods at the beginning and end of the frequency event. The powers delivered to the system for the second type of tests are shown in Fig. 6. This reflects that there are hardly any differences between the powers for the different T_p values evaluated, both in steady- and transient-state. In fact, all the responses can be considered identical to the case of $k_p = 0.075$ of the first group of tests. The same analysis can be carried out on the UC voltage evolution represented in the top plot of Fig. 7. Similar UC voltage evolution for the different values of T_p are observed because they all release practically the same power from the UC. These results reflect that the power losses compensation has more influence on the steady-state, maintaining the UC SoC close to its setpoint, than during the AS provision. This is because the increase in power losses during the provision of the AS is not very significant with respect to the total power delivered to the grid. Regarding the control of the DC bus voltage, illustrated in the bottom plot of Fig. 7, a similar evolution is observed for any value of T_p. An adequate tracking of the reference and a good dynamic response during the beginning and end of the frequency event is achieved in each case.

IV. Conclusions

This paper has presented a EMS of a CI-DRES comprising an UC, where the DC bus voltage of the CI-DRES and the

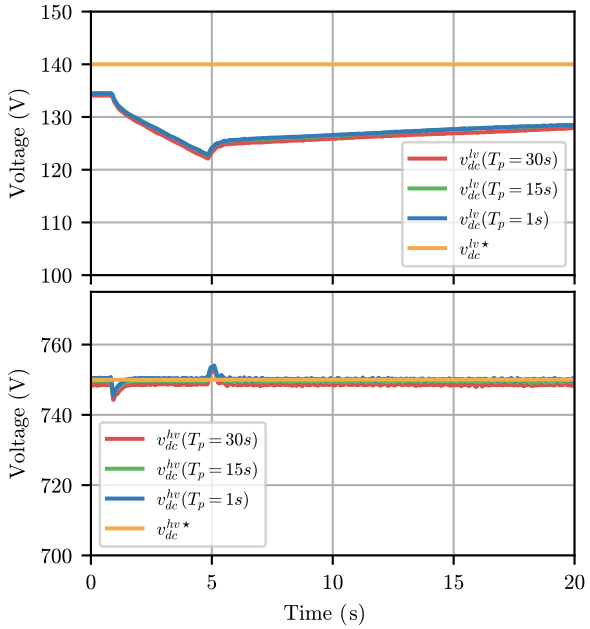

Fig. 7. Voltages of the second group of tests. Top plot: UC voltage evolution for different LPF time constant T_p. Bottom plot: DC voltage bus evolution for different LPF time constant T_p.

UC SoC are controlled simultaneously when the CI-DRES provides an AS. To achieve this, a three-level hierarchical control structure is proposed: UC current control loop, DC bus voltage control loop and UC voltage control loop. The first two control loops correspond to a classic cascade control and are used to control the DC bus voltage. Meanwhile, the third control loop aims to maintain the UC voltage within the technical limits and, simultaneously, must not interfere with the power required by a given AS. For this, two actions are carried out: i) a proportional controller applied to the squared error of the UC voltage and, ii) a power losses compensation through an LPF. After the provision of the AS, the UC must have the ability to return to its reference voltage in order to be able to provide the required AS again in the future.

The proposal was experimentally validated via two types of tests in order to examine how the proportional controller of the UC voltage and the LPF time constant for the power losses compensation affect the ASs provision and the UC voltage. In all examined cases, a good tracking and a fast dynamic response is achieved with respect to the DC voltage bus control. Finally, it has been demonstrated that the control of the DC voltage bus is independent of the proportional controller and the LPF time constant of the third control level.

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