Medium Voltage to Low Voltage Load Flow Algorithm for Unbalanced Islanded Microgrids

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***Abstract*—In this paper, a load flow algorithm for unbalanced islanded Microgrids (MGs) is developed considering both the multigrounded low voltage (LV) and the medium voltage (MV) network. The method is based on the implicit Z_{BUS} load flow method and it can be applied even in highly meshed MGs regardless of the R/X ratio of lines. It presents fast convergence, low computation time and high robustness. In our analysis we consider a variety of transformer configurations and step voltage regulators. Simulations were conducted in IEEE 4-nodes, 6-nodes and in a highly meshed network of 749 MV and LV nodes.**

***Index Terms*—Islanded Microgrids, Load flow, Voltage regulators, Transformers, Multigrounded Grids.**

I. Introduction

Load flow algorithms need to consider both the LV and the MV networks for more accurate results [2]. Although a variety of three phase load flow algorithms has been presented in literature, the overwhelming majority examines only one voltage level [1]. To the author's knowledge, only a few research works exist in literature examining the integration of MV and LV networks into a single load flow problem [2]-[5]. The challenges of such an attempt are mainly the complex modeling of transformer in the load flow problem and the computational complexity arising from a load flow of multiple voltage levels.

Authors in [2] integrated the 3 wire MV and the 4 wire multigrounded LV network into a unified model. Authors in [3] solved the load flow problem from LV up to MV level using a modified backward forward sweep method, while in [4] the authors applied a direct load flow approach and a detailed modeling of a Dyn11 transformer. In [5], the load flow was solved in common αβ0 stationary reference for both MV and LV network. However all the above studies are referred to grid connected networks considering a slack bus in the MV side.

As far as the authors know, there is no method so far for solving the power flow problem from LV up to MV level in islanded MGs. Islanded MGs need a more sophisticated treatment comparing to the traditional networks due to 1) the absence of a slack bus 2) the droop control of DGs and 3) the variation of the frequency which in turn affects the line impedance. The scope of this work is to present a complete model for calculating the load flow in islanded MGs from LV up to MV voltage level, considering the neutral and grounding of LV network, different transformer configurations and step voltage regulators.

II. Load flow algorithm for islanded MGs

The full configuration of an islanded MV MG including the transformers and the virtual slack node as well as of an LV network including the slack node, loads and the multigrounded neutral conductor is shown in Fig. 1a and 1b respectively. The nodal admittance matrix of the islanded MV network with m nodes is described by (1), where the notation 0 corresponds to the virtual slack node. It is noted that the virtual slack node is connected to a random node of the network through freely selected impedances (e.g. Z_{01}^{A}).

$$\begin{bmatrix} I_0 \\ I_1 \\ \dots \\ I_m \end{bmatrix} = \begin{bmatrix} Y_{00} & Y_{01} & \cdots & Y_{0m} \\ Y_{10} & Y_{11} & \cdots & Y_{1m} \\ \vdots & \vdots & \cdots & \vdots \\ Y_{m0} & Y_{m1} & \cdots & Y_{mm} \end{bmatrix} \cdot \begin{bmatrix} V_0 \\ V_1 \\ \dots \\ V_m \end{bmatrix} \tag{1}$$

In order to formulate the final equations of the load flow problem we initially remove the first three rows of (1) corresponding to the currents of virtual slack bus. Thus (2) is derived as follows:

$$I_{new} = Y_{new} \cdot V \tag{2}$$

where $V=[V_0, V_1, \dots, V_m]^T$ consists of network voltages, Y_{new} is the modified admittance matrix and $I_{new}=[I_1, \dots, I_m]^T$.

Lastly, we define the final matrices Y'_{fin} and Y_{fin}. The first one consists of the first three columns of Y_{new}, while the second one consists of all the other columns of Y_{new} so that $Y_{new} = [Y'_{fin} \;\; Y_{fin}.]$. Using this modification, (2) is transformed to (3), where $V_{fin}= [V_1, \dots, V_m]$ and k is the iteration number:

$$Y_{fin}^{-1} \cdot \left[-Y'_{fin} \cdot V_0 + I_{new} \right]^k = V_{fin}^{k+1} \tag{3}$$

Equation (3) calculates iteratively the voltages of all the nodes (except the virtual slack node) as a function of the load currents, the voltage of the virtual slack node at the previous iteration as well as the matrices Y'_{fin} and Y_{fin}.

In islanded MV networks, the DGs operate in droop control mode as expressed by (4):

$$f = f_{0i} - K_{Pi} \cdot P_{Gi} \tag{4a}$$

$$\left|V_i^1\right| = \left|V_{0i}\right| - K_{Qi} \cdot Q_{Gi} \tag{4b}$$

where f, f_{0i}, K_{pi}, P_{Gi}, V_i^1, V_{0i}, K_{Qi} and Q_{Gi} are the output frequency, nominal frequency, frequency droop gain, active power output, positive sequence voltage magnitude, nominal voltage, voltage droop gain and reactive power output of DG unit i, respectively. In order to accommodate the particularities of islanded MV networks, the frequency of the network is updated in each iteration as in (5a), so that the power flowing through the virtual slack node (P_{slack}) is nullified. Please note, that P_{slack} is dependent on the DGs active power and therefore on the frequency through (4a). Furthermore, the voltage of virtual slack node is set equal at each iteration with its adjacent node as shown in (5b). After the algorithm has converged, the virtual slack node has acquired the same voltage as its adjacent node, thus it is as if it does not exist.

$$f^{k+1} = f^k + \frac{P_{slack}^{\;k}}{\sum_{i=1}^{m} \frac{1}{K_{pi}}} \tag{5a}$$

$$\begin{vmatrix} V_{(0,A)} \\ V_{(0,B)} \\ V_{(0,C)} \end{vmatrix}^{k+1} = \begin{vmatrix} V_{(1,A)} \\ V_{(1,B)} \\ V_{(1,C)} \end{vmatrix}^{k} \tag{5b}$$

The LV grid is solved using as slack node the secondary side of transformers, the voltage of which is updated in each iteration depending on the solution of the islanded MV grid and the transformer configuration, as referred in section III.

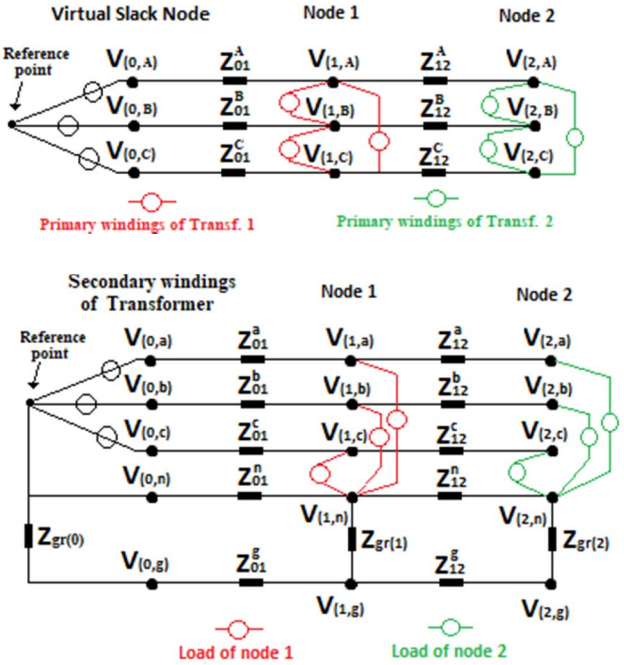

Fig. 1: (a) Islanded MV network with two transformers and the virtual slack node. (b) LV network with one slack node and two load nodes.

III. MODELING OF TRANSFORMERS

Many general models of transformers have been developed for load flow analysis, most of which are based on the primitive admittance matrix [6]. However they use quite complex matrices making the solution of load flow a very sophisticated process [5]. On the other hand, a very simple and accurate method for modeling transformers was proposed in [7], based on the Kirchhoff's current and voltage law in *abc* coordinates, but the authors only described the wye-delta connection.

In this paper, we extend the model of [7] in several commonly used transformer configurations and apply it with the implicit Z_{BUS} method instead of the BFS method of [7]. The transformer model is described by two equations: One for calculating the MV side currents and one for calculating the LV side voltages of the transformer. It is noted, that due to its very large value, the magnetizing impedance can be neglected, without affecting the accuracy of the load flow solution [7][12]. Hence the leakage impedance can be considered in either the MV or LV side of the transformer without affecting the results. The transformer equations for several widely used configurations are quoted below:

A) Ungrounded wye-delta configuration

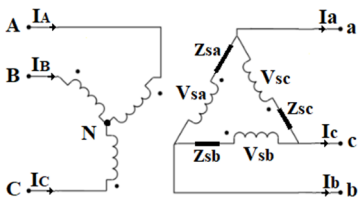

Fig. 2: Ungrounded wye--delta transformer configuration.

An ungrounded wye-delta connection is depicted in Fig. 2 with the leakage impedance included in the secondary side. By considering that $\frac{V_{AN}}{V_{Sa}} = \frac{I_{Sa}}{I_A} = N$ (similar for the other phases) we derive (6), where N is the windings ratio between primary and secondary side.

$$\begin{aligned} V_{AB} &= N \cdot V_{sa} - N \cdot V_{sb} \\ V_{BC} &= N \cdot V_{sb} - N \cdot V_{sc} \\ V_{sa} + V_{sb} + V_{sc} - N \cdot I_A \cdot Z_{sa} - N \cdot I_B \cdot Z_{sb} - N \cdot I_C \cdot Z_{sc} &= 0 \end{aligned} \tag{6}$$

The phase-to-phase voltages of delta connection can be written as a function of V_{sa}, V_{sb}, and V_{sc} as follows:

$$\begin{aligned} V_{ab} &= V_{sa} - N \cdot I_A \cdot Z_{sa} \\ V_{bc} &= V_{sb} - N \cdot I_B \cdot Z_{sb} \\ V_{ca} &= V_{sc} - N \cdot I_C \cdot Z_{sc} \end{aligned} \tag{7}$$

By combining equation systems (6) and (7), (8) is obtained for calculating the LV voltages of transformers in the forward process for given MV voltages and currents:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = A_1 \cdot \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} + B_1 \cdot \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{8}$$

where

$$A_1 = \begin{bmatrix} \frac{2}{3 \cdot N} & \frac{1}{3 \cdot N} & 0 \\ -\frac{1}{3 \cdot N} & \frac{1}{3 \cdot N} & 0 \\ -\frac{1}{3 \cdot N} & -\frac{2}{3 \cdot N} & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} -\frac{2 \cdot N \cdot Z_{sa}}{3} & \frac{2 \cdot N \cdot Z_{sa}}{3} - \frac{N \cdot Z_{sb}}{3} & \frac{N \cdot Z_{sc}}{3} \\ \frac{N \cdot Z_{sa}}{3} & -\frac{N \cdot Z_{sa}}{3} - \frac{N \cdot Z_{sb}}{3} & \frac{N \cdot Z_{sc}}{3} \\ \frac{N \cdot Z_{sa}}{3} & \frac{2 \cdot N \cdot Z_{sb}}{3} - \frac{N \cdot Z_{sa}}{3} & -\frac{2 \cdot N \cdot Z_{sc}}{3} \end{bmatrix}$$

The MV transformer currents are obtained from the LV currents of transformers in the backward process as follows:

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{1}{3 \cdot N} & -\frac{1}{3 \cdot N} \\ \frac{1}{3 \cdot N} & \frac{2}{3 \cdot N} \\ -\frac{2}{3 \cdot N} & -\frac{1}{3 \cdot N} \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \end{bmatrix} \tag{9}$$

B) Delta-grounded wye configuration

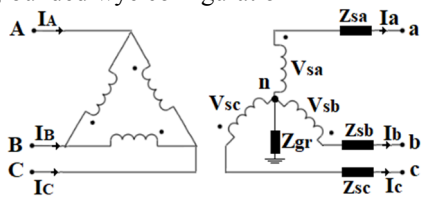

Fig. 3: Delta-Grounded wye transformer configuration. The leakage impedances are included in the secondary side of the transformer.

The LV voltages in forward process are obtained by (10):

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = A_2 \cdot \begin{bmatrix} V_{AC} \\ V_{BA} \\ V_{CB} \end{bmatrix} + B_2 \cdot \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{10}$$

where

$$A_2 = \begin{bmatrix} \frac{1}{N} & 0 & 0 \\ 0 & \frac{1}{N} & 0 \\ 0 & 0 & \frac{1}{N} \end{bmatrix} \qquad B_2 = \begin{bmatrix} -Z_{sa} & 0 & 0 \\ 0 & -Z_{sb} & 0 \\ 0 & 0 & -Z_{sc} \end{bmatrix}$$

The MV transformer currents are obtained from the LV currents of transformers in the backward process as follows:

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{1}{N} & -\frac{1}{N} & 0 \\ 0 & \frac{1}{N} & -\frac{1}{N} \\ -\frac{1}{N} & 0 & \frac{1}{N} \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{11}$$

C) Delta-delta configuration

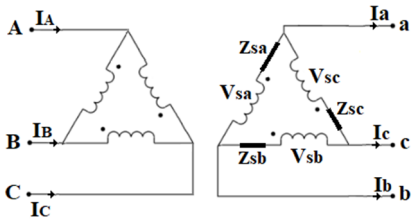

Fig. 4: Delta-delta transformer configuration. The leakage impedances are included in the secondary side of the transformer

The LV voltages in forward process are obtained by (12):

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = A_3 \cdot \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} - B_3 \cdot \begin{bmatrix} I_a \\ I_b \end{bmatrix} \tag{12}$$

where

$$A_3 = \begin{bmatrix} \frac{1}{N} & 0 & 0 \\ 0 & \frac{1}{N} & 0 \\ 0 & 0 & \frac{1}{N} \end{bmatrix}$$

$$B_3 = \begin{bmatrix} \frac{Z_{sa} \cdot Z_{sc}}{Z_{sa}+Z_{sb}+Z_{sc}} & \frac{-Z_{sa} \cdot Z_{sb}}{Z_{sa}+Z_{sb}+Z_{sc}} \\ \frac{Z_{sb} \cdot Z_{sc}}{Z_{sa}+Z_{sb}+Z_{sc}} & \frac{Z_{sb} \cdot (Z_{sa}+Z_{sc})}{Z_{sa}+Z_{sb}+Z_{sc}} \\ \frac{-Z_{sc} \cdot (Z_{sa}+Z_{sb})}{Z_{sa}+Z_{sb}+Z_{sc}} & \frac{-Z_{sb} \cdot Z_{sc}}{Z_{sa}+Z_{sb}+Z_{sc}} \end{bmatrix}$$

The MV transformer currents are obtained from the LV currents of transformers in the backward process as follows:

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{(Z_{sa}+Z_{sb}+Z_{sc})}{N \cdot (Z_{sa}+Z_{sb}+Z_{sc})} & 0 \\ 0 & \frac{(Z_{sa}+Z_{sb}+Z_{sc})}{N \cdot (Z_{sa}+Z_{sb}+Z_{sc})} \\ \frac{-(Z_{sa}+Z_{sb}+Z_{sc})}{N \cdot (Z_{sa}+Z_{sb}+Z_{sc})} & \frac{-(Z_{sa}+Z_{sb}+Z_{sc})}{N \cdot (Z_{sa}+Z_{sb}+Z_{sc})} \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \end{bmatrix} \tag{13}$$

D) Grounded wye-grounded wye

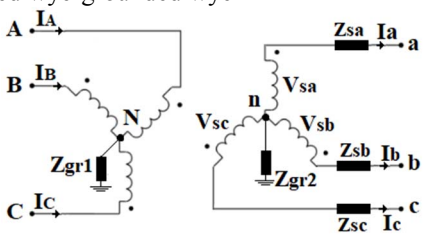

Fig. 5: Grounded wye-grounded wye transformer configuration.

The LV voltages in forward process are obtained by (14):

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = A_4 \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} - B_4 \cdot \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{14}$$

where

$$A_4 = \begin{bmatrix} \frac{1}{N} & 0 & 0 \\ 0 & \frac{1}{N} & 0 \\ 0 & 0 & \frac{1}{N} \end{bmatrix} \quad B_4 = \begin{bmatrix} Z_{sa} \cdot N + \frac{Z_{gr1}}{N} & \frac{Z_{gr1}}{N} & \frac{Z_{gr1}}{N} \\ \frac{Z_{gr1}}{N} & Z_{sb} \cdot N + \frac{Z_{gr1}}{N} & \frac{Z_{gr1}}{N} \\ \frac{Z_{gr1}}{N} & \frac{Z_{gr1}}{N} & Z_{sc} \cdot N + \frac{Z_{gr1}}{N} \end{bmatrix}$$

The MV transformer currents are obtained from the LV currents of transformers in the backward process as follows:

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{1}{N} & 0 & 0 \\ 0 & \frac{1}{N} & 0 \\ 0 & 0 & \frac{1}{N} \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{15}$$

E) Grounded wye-delta

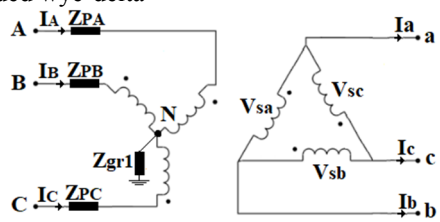

Fig. 6: Grounded wye-delta transformer configuration. The leakage impedances are included in the primary side of the transformer.

The LV voltages in forward process are obtained by (16):

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = A_5 \cdot \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} + B_5 \cdot \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{16}$$

where

$$A_5 = \begin{bmatrix} \frac{2}{3 \cdot N} & \frac{1}{3 \cdot N} & 0 \\ -\frac{1}{3 \cdot N} & \frac{1}{3 \cdot N} & 0 \\ -\frac{1}{3 \cdot N} & -\frac{2}{3 \cdot N} & 0 \end{bmatrix} \quad B_5 = \begin{bmatrix} -\frac{2 \cdot Z_{PA}}{3 \cdot N} & \frac{Z_{PB}}{3 \cdot N} & \frac{Z_{PC}}{3 \cdot N} \\ \frac{Z_{PA}}{3 \cdot N} & -\frac{2 \cdot Z_{PB}}{3 \cdot N} & \frac{Z_{PC}}{3 \cdot N} \\ \frac{Z_{PA}}{3 \cdot N} & \frac{Z_{PB}}{3 \cdot N} & -\frac{2 \cdot Z_{PC}}{3 \cdot N} \end{bmatrix}$$

In the case of grounded wye-delta connection, the circulating current of delta connection is not zero as occurs in the case of ungrounded wye-delta configuration, because there is zero-sequence current component in the MV side of transformer flowing through the grounding resistance. Hence, in order to specify the MV transformer currents based on the LV transformer currents, we need firstly to estimate the circulating current inside the delta connection.

$$\begin{aligned} V_A - I_A \cdot Z_{PA} - V_{PA} &= (I_A + I_B + I_C) \cdot Z_{gr} \\ V_B - I_B \cdot Z_{PB} - V_{PB} &= (I_A + I_B + I_C) \cdot Z_{gr} \\ V_C - I_C \cdot Z_{PC} - V_{PC} &= (I_A + I_B + I_C) \cdot Z_{gr} \end{aligned} \tag{17}$$

By adding equations (17) with each other and considering that $\frac{I_{sa}}{I_A} = \frac{I_{sb}}{I_B} = \frac{I_{sc}}{I_C} = N$, $\frac{Z_{PA}}{Z_{sa}} = \frac{Z_{PB}}{Z_{sb}} = \frac{Z_{PC}}{Z_{sc}} = N^2$ and $V_{PA}+V_{PB}+V_{PC}= V_{sa}+V_{sb}+V_{sc}=0$ we derive (18):

$$\begin{bmatrix} I_a \\ I_b \\ V_A + V_B + V_C \end{bmatrix} = \begin{bmatrix} N & 0 & -N \\ -N & N & 0 \\ 3 \cdot Z_{gr} + N^2 \cdot Z_{sa} & 3 \cdot Z_{gr} + N^2 \cdot Z_{sb} & 3 \cdot Z_{gr} + N^2 \cdot Z_{sc} \end{bmatrix} \cdot \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{18}$$

From (18) we finally obtain (19) by inverting the square matrix. As shown in (19), the MV currents of transformer are calculated by the LV side currents and the MV voltages.

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} N & 0 & -N \\ -N & N & 0 \\ 3\cdot Z_{gr} + N^2 \cdot Z_{sa} & 3\cdot Z_{gr} + N^2 \cdot Z_{sb} & 3\cdot Z_{gr} + N^2 \cdot Z_{sc} \end{bmatrix}^{-1} \cdot \begin{bmatrix} I_a \\ I_b \\ V_A + V_B + V_C \end{bmatrix} \tag{19}$$

The load flow problem is solved sequentially by applying the implicit Z_{BUS} firstly at the LV networks where we calculate the currents at the LV side of the transformer. From the LV currents we specify the currents at the MV side of the transformer by implementing the transformer model described in this section. Subsequently, we solve the load flow in the MV network using the proposed algorithm for islanded networks. After we have solved the load flow in MV network we use the transformer model to calculate the voltage at the LV side of the transformer which is considered as the slack bus of LV network. The process is iteratively executed until the final convergence. It is noted that the reference points for MV and LV networks (in wye configuration) are shown in Fig. 1. The reference point of LV networks in delta configuration is one of a, b or c points of Figs. 2, 4, 6.

IV. Modeling of Step Voltage Regulators

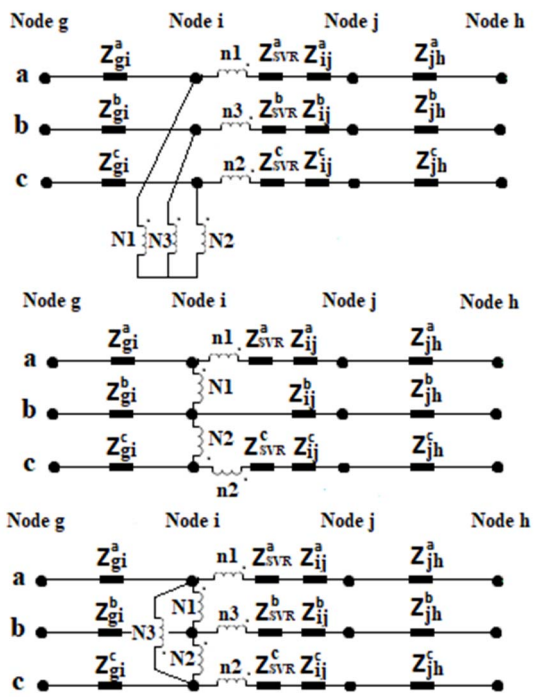

Fig. 7: Type A SVR configurations with turn ratios of each autotransformer equal to N1:n1, N2:n2, N3:n3: From top to bottom: a) Wye configuration, b) Open delta configuration, c) Close Delta configuration.

Step voltage regulators (SVR) are devices that are designed to keep the voltage of the network within permissible limits and are usually connected in wye, open-delta or close-delta configuration. The connection of all types of SVR is shown in Fig. 7. The leakage impedance of each autotransformer is considered in series with the series windings (e.g n1, n2, n3). The present model for SVR can be applied in both type A and type B SVR connections, since only the position of series winding differs between the two types. More specifically, in type B, the series winding is connected between nodes i and g according to Fig. 7 instead of *i* and *j*. Therefore, the only change in mathematical equations below would be *j* replaced by *g,* if a type B SVR was modeled.

The current vector of node *i* includes both the load current and the current vector of shunt winding of SVR as shown in (20).

$$\boldsymbol{I_i} = \begin{bmatrix} I^a_{i,SVR} & I^b_{i,SVR} & I^c_{i,SVR} \end{bmatrix}^T + \begin{bmatrix} I^a_{i,L} & I^b_{i,L} & I^c_{i,L} \end{bmatrix}^T \tag{20}$$

The series winding of SVR is connected between the node i and j as shown in Fig. 7. The current vector of node j is expressed by (21) including only the current vector of the load that is connected to this node.

$$\boldsymbol{I_j} = \begin{bmatrix} I^a_{j,L} & I^b_{j,L} & I^c_{j,L} \end{bmatrix}^T \tag{21}$$

The currents of nodes i and j are expressed as a function of the node voltages and line admittances by (22) and (23):

$$\boldsymbol{I_i} = \boldsymbol{Y_{ig}} \cdot (\boldsymbol{V_g} - \boldsymbol{V_i}) + \boldsymbol{Y'_{ij}} \cdot (\boldsymbol{V_j} - \boldsymbol{V'_i}) \tag{22}$$

$$\boldsymbol{I_j} = \boldsymbol{Y_{jh}} \cdot (\boldsymbol{V_h} - \boldsymbol{V_j}) + \boldsymbol{Y'_{ij}} \cdot (\boldsymbol{V'_i} - \boldsymbol{V_j}) \tag{23}$$

In (22) and (23), the $\boldsymbol{V'_i}$ is given by (24), where I is the identity matrix while K is given by Table I of Appendix for every SVR configuration regardless of the type of SVR.

$$\boldsymbol{V'_i} = (\boldsymbol{K} + \boldsymbol{I}) \cdot \boldsymbol{V_i} \tag{24}$$

The current vector of shunt winding of SVR of (20) is given by (25), based on the relation between the currents between shunt and series windings of autotransformers.

$$\boldsymbol{I_{i,SVR}} = \boldsymbol{A_a} \cdot \boldsymbol{Y'_{ij}} \cdot (\boldsymbol{V_j} - \boldsymbol{V'_i}) \tag{25}$$

Combining (20), (22) and (25) we obtain (26). Equations (23) and (26) express the load current vector of nodes j and i respectively. The SVR current vector of (20) has been transferred at the right hand side of (22).

$$\boldsymbol{I_{i,L}} = \boldsymbol{Y_{ig}} \cdot (\boldsymbol{V_g} - \boldsymbol{V_i}) + (\boldsymbol{I} - \boldsymbol{A_a}) \cdot \boldsymbol{Y'_{ij}} \cdot (\boldsymbol{V_j} - \boldsymbol{V'_i}) \tag{26}$$

Finally, by applying (24) and (27) into (26) as well as (24) and (28) into (23) we obtain the final equations (29) and (30), which express the load current vectors as a function of the node voltage vectors.

$$\boldsymbol{F_i} = (\boldsymbol{I} - \boldsymbol{A_a}) \cdot \boldsymbol{Y'_{ij}} - \boldsymbol{Y_{ij}} \tag{27}$$

$$\boldsymbol{F_j} = \boldsymbol{Y'_{ij}} - \boldsymbol{Y_{ij}} \tag{28}$$

$$\boldsymbol{I_{i,L}} = \boldsymbol{Y_{ig}} \cdot (\boldsymbol{V_g} - \boldsymbol{V_i}) + \boldsymbol{Y_{ij}} \cdot (\boldsymbol{V_j} - \boldsymbol{V_i}) - (\boldsymbol{Y_{ij}} \cdot \boldsymbol{K} + \boldsymbol{F_i} + \boldsymbol{K} \cdot \boldsymbol{F_i}) \cdot \boldsymbol{V_i} + \boldsymbol{F_i} \cdot \boldsymbol{V_j} \tag{29}$$

$$\boldsymbol{I_{j,L}} = \boldsymbol{Y_{jh}} \cdot (\boldsymbol{V_h} - \boldsymbol{V_j}) + \boldsymbol{Y_{ij}} \cdot (\boldsymbol{V_i} - \boldsymbol{V_j}) + (\boldsymbol{Y_{ij}} \cdot \boldsymbol{K} + \boldsymbol{F_j} + \boldsymbol{K} \cdot \boldsymbol{F_j}) \cdot \boldsymbol{V_i} - \boldsymbol{F_j} \cdot \boldsymbol{V_j} \tag{30}$$

It is noted that $\boldsymbol{I_{i,L}} = \boldsymbol{Y_{ig}} \cdot (\boldsymbol{V_g} - \boldsymbol{V_i}) + \boldsymbol{Y_{ij}} \cdot (\boldsymbol{V_j} - \boldsymbol{V_i})$ and $\boldsymbol{I_{j,L}} = \boldsymbol{Y_{jh}} \cdot (\boldsymbol{V_h} - \boldsymbol{V_j}) + \boldsymbol{Y_{ij}} \cdot (\boldsymbol{V_i} - \boldsymbol{V_j})$ express the current equations of bus admittance matrix as if no SVR is connected between nodes i and j. The terms $(\boldsymbol{Y_{ij}} \cdot \boldsymbol{K} + \boldsymbol{F_i} + \boldsymbol{K} \cdot \boldsymbol{F_i}) \cdot \boldsymbol{V_i} + \boldsymbol{F_i} \cdot \boldsymbol{V_j}$ and $(\boldsymbol{Y_{ij}} \cdot \boldsymbol{K} + \boldsymbol{F_j} + \boldsymbol{K} \cdot \boldsymbol{F_j}) \cdot \boldsymbol{V_i} - \boldsymbol{F_j} \cdot \boldsymbol{V_j}$ are the additional terms that simply need to be added into bus admittance matrix in order to include the SVR operation. The matrices $\boldsymbol{Y'_{ij}}$, $\boldsymbol{K}$, $\boldsymbol{A_a}$ are given in Table I of Appendix.

V. Proposed Load Flow Method Validation

In order to validate the proposed algorithm in unbalanced islanded operation of MGs, a comparison is carried out with the time-domain environment of MALAB/Simulink. To reduce the simulation time of the time-consuming environment of Simulink, DGs are simulated as ideal droop-controlled balanced voltage sources, neglecting the high-order PWM harmonics

produced by the DG converters. The comparison is executed using the 6-Bus LV network of Fig. 8 in islanded mode, with the parameters of Table I, considering the neutral and grounding conductors of LV network. To treat the islanding effect, the virtual slack bus concept and the variation of frequency according to (5) was applied in the network. The results are depicted in Table II and they are in full agreement with the ones of Simulink. However, the proposed method offers a significant simulation time reduction. For the sake of fairness, all the simulations were executed in a 64-bit laptop with processor Intel Core i5-6300HQ, 3.2GHz, 8GB RAM.

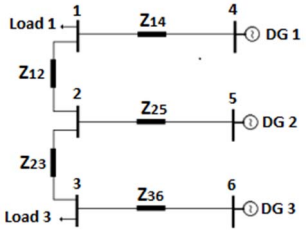

Fig. 8. Islanded grid of 6-Buses with 3 DG units and 2 PQ-Nodes.

TABLE I
PARAMETERS OF UNBALANCED NETWORK

Resistance of the lines	0.5 Ohm/km
Self-Reactance of the lines	0.6 mH/km
Mutual-Reactance of the lines	0.1 mH/km
Line lengths	0.1 km
Loads of PQ nodes	See table IV
K_{Pi} **(*i*=4, 5, 6)**	$5\cdot10^{-6}$ (Hz/W)
K_{Qi} **(*i*=4, 5, 6)**	$2\cdot10^{-4}$ (V/VAR)
V_{0i} **(*i*=4, 5, 6)**	230 V
f_{0i} **(*i*=4, 5, 6)**	50 Hz
Ground resistances	25 Ohm

TABLE II
COMPARATIVE RESULTS FOR THE ISLANDED 6-BUS UNBALANCED MG

Node-Phase	Phase-Neutral Volt.		P (W)		Q (VAR)	
	Proposed	Simulink	Proposed	Simulink	Proposed	Simulink
1a	227.5087	227.5086	5000	5000	3750	3750
1b	227.8351	227.8349	4000	4000	3000	3000
1c	228.5305	228.5301	3000	3000	2250	2250
2a	228.0076	228.0075	0	0	0	0
2b	228.2254	228.2249	0	0	0	0
2c	228.6889	228.6889	0	0	0	0
3a	227.5087	227.5086	5000	5000	3750	3750
3b	227.8351	227.8349	4000	4000	3000	3000
3c	228.5305	228.5301	3000	3000	2250	2250
4a	228.6932	228.6932	-3443.8	-3443.8	-2740.6	-2740.6
4b	228.6932	228.6932	-2677	-2677	-2183.4	-2183.4
4c	228.6932	228.6932	-1920	-1920	-1610	-1610
5a	229.0059	229.0059	-3190	-3190	-2032.5	-2032.5
5b	229.0059	229.0059	-2678.1	-2678.1	-1660.4	-1660.4
5c	229.0059	229.0059	-2172.7	-2172.7	-1277.6	-1277.6
6a	228.6932	228.6932	-3443.8	-3443.8	-2740.6	-2740.6
6b	228.6932	228.6932	-2677	-2677	-2183.4	-2183.4
6c	228.6932	228.6932	-1920	-1920	-1610	-1610
MG frequency: Proposed: f = 49.9598 Hz, Simulink: f = 49.9598 Hz						
Execution time: Proposed: Δt = 0.068 sec, Simulink: Δt = 180 sec						

VI. TRANSFORMER MODEL VALIDATION

In order to investigate the convergence of the proposed transformer model when applied with the implicit Z_{BUS} method, simulations were executed in Matlab using the IEEE 4 bus test network [8]. Table III illustrates the number of iterations for several transformer models so that they converge with an accuracy of 10^{-5} pu. It is noted that, the results of Table III are from [9]. As shown, the proposed transformer model applied with the implicit Z_{BUS} load flow method presents the fastest convergence. The transformer models of [9] and [6] have been applied with the BFS method, while the model of [10] with the implicit Z_{BUS} method.

TABLE III
COMPARISON OF THE CONVERGENCE BETWEEN THE PROPOSED MODEL AND MODELS OF REF. [6], [9], [10] FOR THE IEEE 4 NODE GRID

	Iteration number per method			
	Ref. [9]	Ref. [10]	Ref. [6]	Proposed
Y_g - Y_g	13	13	18	13
Y_g - Δ	8	divergence	9	7
Y - Δ	8	divergence	9	6
Δ - Y_g	21	divergence	16	11
Δ - Δ	7	16	9	7

VII. CASE STUDY INVESTIGATION

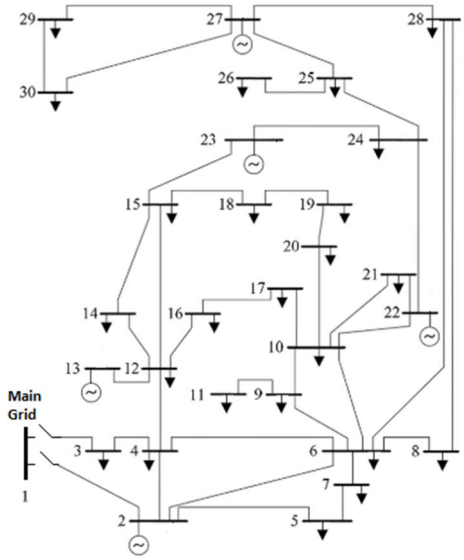

Fig. 9. 30-Bus MV islanded network. The topology of the network is from [11]. Line parameters were modified to represent typical MV parameters.

To test the computation performance and robustness of the proposed load flow approach, a meshed network consisting of 29 islanded MV nodes was used, with the configuration shown in Fig. 9. Every load node of MV network is connected through a delta-grounded wye transformer to an LV sub-network of the same configuration (as Fig. 9). In all LV sub-networks the transformer is connected to bus 1. An SVR of open delta configuration is connected between the nodes 24-25 in the MV network. The parameters of MV and LV networks are depicted in Table IV. Simulations were executed in Matlab using a 64-bit laptop with processor Intel Core i5-6300HQ, 3.2GHz, 8GB RAM. The algorithm converges with an accuracy of 10^{-4} V after 0.51 seconds. Given the large size of the network (749 Nodes) and high accuracy of the method, this computation time confirms that the proposed method is a sufficient tool for solving in real time the load flow of unbalanced islanded networks involving different voltage levels, while considering the neutral and ground effects of LV networks.

Fig. 10a depicts the phase to phase voltage of all MV nodes of the network. As shown, the voltage of MV network varies from node to node. For example, the SVR connected between the nodes 24-25 causes a voltage rise of about 0.75kV. This voltage rise is transferred to LV subgrids through the MV/LV transformer. Hence, for more accurate results of load flow in LV networks, the MV voltages should be also taken into consideration.

The majority of load flow methods so far, ignore completely the neutral and grounding conductors or hide them using Kron's reduction. This is not a correct assumption in LV networks, where the neutral conductor has a non zero voltage. To highlight it, two different grounding resistance values were considered in the LV subgrid that is supplied by MV node 30 of Fig. 9. In LV networks, the loads are usually connected between phase and neutral. Assuming a perfect multigrounded grid (namely zero neutral voltage) the phase to neutral voltages of LV network are shown in Fig. 10b. On the other hand, considering the grounding resistances equal to 25Ωhm, the phase to neutral voltages of the same subgrid are shown in Fig. 10c. The big difference between the two figures resulted from the voltage of neutral conductor, which can be added or subtracted from the phase voltage. As a result, the explicit consideration of neutral and ground conductors in LV networks is necessary.

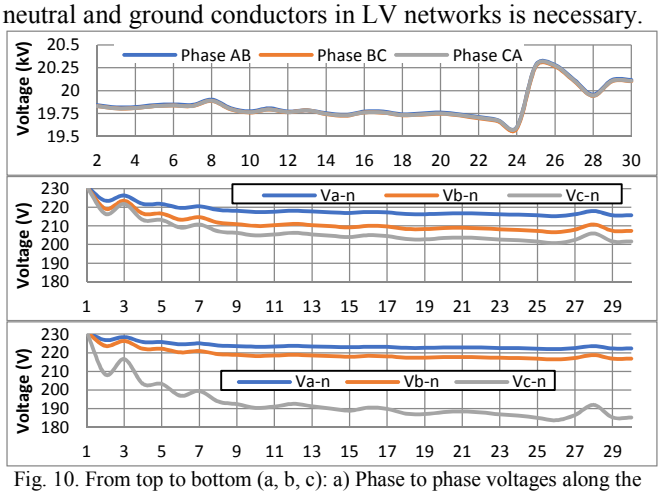

Fig. 10. From top to bottom (a, b, c): a) Phase to phase voltages along the MV network. b) Phase to neutral voltages of LV subgrid supplied by the MV node 30. The neutral conductor is neglected. c) The neutral conductor is considered. Horizontal axis denote node No.

TABLE IV

PARAMETERS OF MV (LV)* NETWORKS

*MV parameters are with bold letters, while LV parameters with normal letters inside the parenthesis.

Resistance of the lines	**0.161** (0.642) Ohm/km
Self-Reactance of the lines	**0.19** (0.083) mH/km
Mutual-Reactance of the lines	**0.05** (0.05) mH/km
Line lengths	**1** (0.1) km
LV loads per node. Phase (A, B, C)	(1.5, 2, 2.5) KW
Power factor of loads (cosφ)	(0.8)
K_{Pi} (i=2, 13, 22, 23, 27)	**$5\cdot10^{-6}$ Hz/W**
K_{Qi} (i=2, 13, 22, 23, 27)	**$2\cdot10^{-4}$ V/VAR**
V_{0i} (i=2, 13, 22, 23, 27)	**20 kV**
f_{0i} (i=2, 13, 22, 23, 27)	**50 Hz**
Transformers ratio	20/0.4 kV
SVR ratio: n1/N1, n2/N2	**0.05**, **0.05**

VIII. CONCLUSION

This paper presented a load flow approach for islanded unbalanced networks, involving different voltage levels. Furthermore, an approach for modeling transformers and step voltage regulators of different configurations was presented. The proposed load flow method is based on the implicit Z_{BUS} method, thus presents fast convergence with low computation time and high robustness. The results confirmed that the proposed method can be applied in real time to calculate the load flow problem of large islanded networks, considering explicitly the neutral conductor and ground of LV networks for more precise results.

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APPENDIX

TABLE I

SVR PARAMETERS FOR SEVERAL CONFIGURATIONS

	Wye configuration	Closed-Delta configuration	Open-Delta configuration
Y'_{ij}	$\begin{bmatrix} Y_{ij}^{aa}+Z_{SVR}^{a\ -1} & Y_{ij}^{ab} & Y_{ij}^{ac} \\ Y_{ij}^{ab} & Y_{ij}^{bb}+Z_{SVR}^{b\ -1} & Y_{ij}^{bc} \\ Y_{ij}^{ac} & Y_{ij}^{bc} & Y_{ij}^{cc}+Z_{SVR}^{c\ -1} \end{bmatrix}$	$\begin{bmatrix} Y_{ij}^{aa}+Z_{SVR}^{a\ -1} & Y_{ij}^{ab} & Y_{ij}^{ac} \\ Y_{ij}^{ab} & Y_{ij}^{bb}+Z_{SVR}^{b\ -1} & Y_{ij}^{bc} \\ Y_{ij}^{ac} & Y_{ij}^{bc} & Y_{ij}^{cc}+Z_{SVR}^{c\ -1} \end{bmatrix}$	$\begin{bmatrix} Y_{ij}^{aa}+Z_{SVR}^{a\ -1} & Y_{ij}^{ab} & Y_{ij}^{ac} \\ Y_{ij}^{ab} & Y_{ij}^{bb} & Y_{ij}^{bc} \\ Y_{ij}^{ac} & Y_{ij}^{bc} & Y_{ij}^{cc}+Z_{SVR}^{c\ -1} \end{bmatrix}$
A_a	$\begin{bmatrix} a_a & 0 & 0 \\ 0 & a_b & 0 \\ 0 & 0 & a_c \end{bmatrix}$	$\begin{bmatrix} a_a & 0 & -a_c \\ -a_a & a_b & 0 \\ 0 & -a_b & a_c \end{bmatrix}$	$\begin{bmatrix} a_a & 0 & 0 \\ -a_a & 0 & -a_c \\ 0 & 0 & a_c \end{bmatrix}$
K	$\begin{bmatrix} a_a & 0 & 0 \\ 0 & a_b & 0 \\ 0 & 0 & a_c \end{bmatrix}$	$\begin{bmatrix} a_a & -a_a & 0 \\ 0 & a_b & -a_b \\ -a_c & 0 & a_c \end{bmatrix}$	$\begin{bmatrix} a_a & -a_a & 0 \\ 0 & 0 & 0 \\ 0 & -a_c & a_c \end{bmatrix}$